

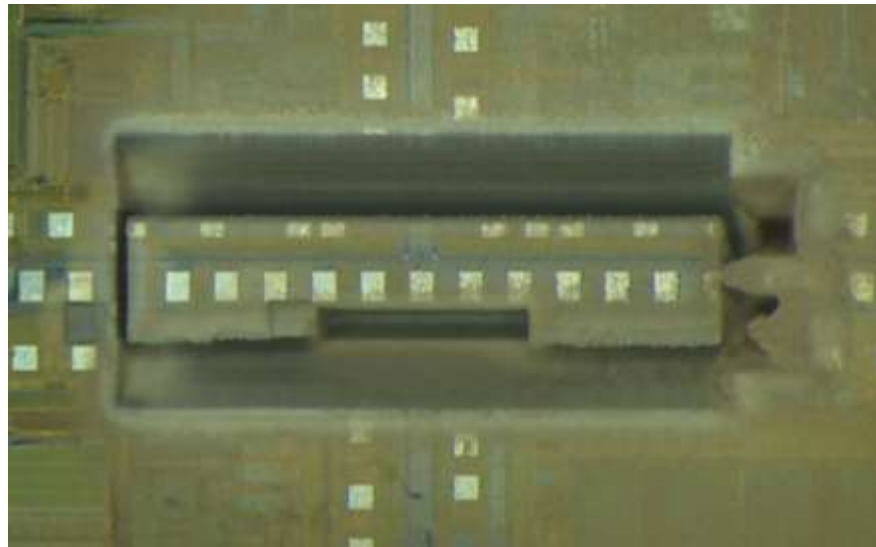
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# Combination of precise laser and FIB milling for TEM based IC failure analysis

EFUG - Workshop, Bordeaux 28<sup>th</sup> September 2017

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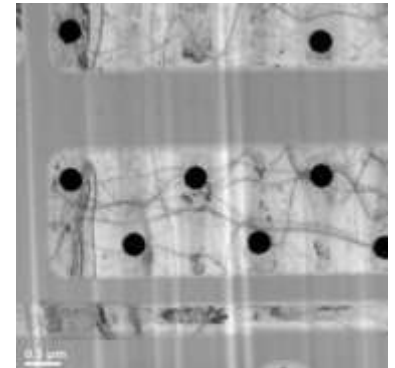
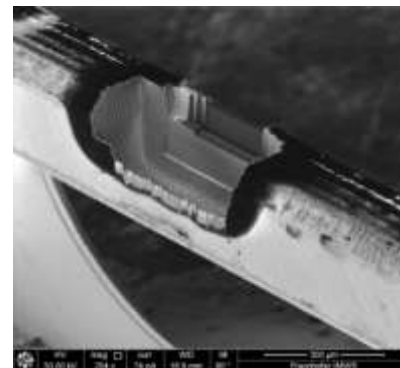
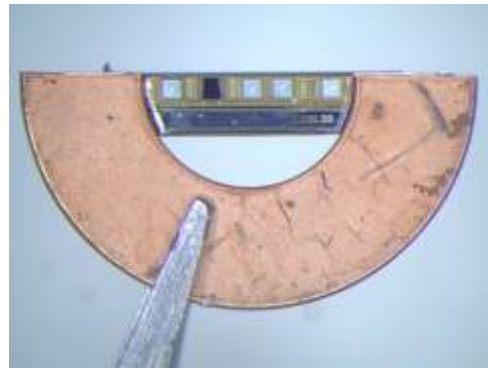
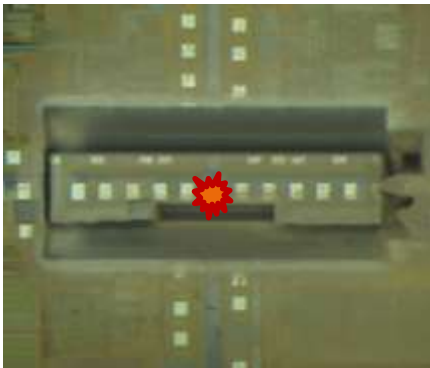
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# Purpose

- Reliable and efficient workflow for planar TEM investigations of IC areas with roughly estimated defect position
- Combination of precise **laser milling** and **Plasma-FIB** to shorten preparation time and get access to large areas for TEM defect inspection



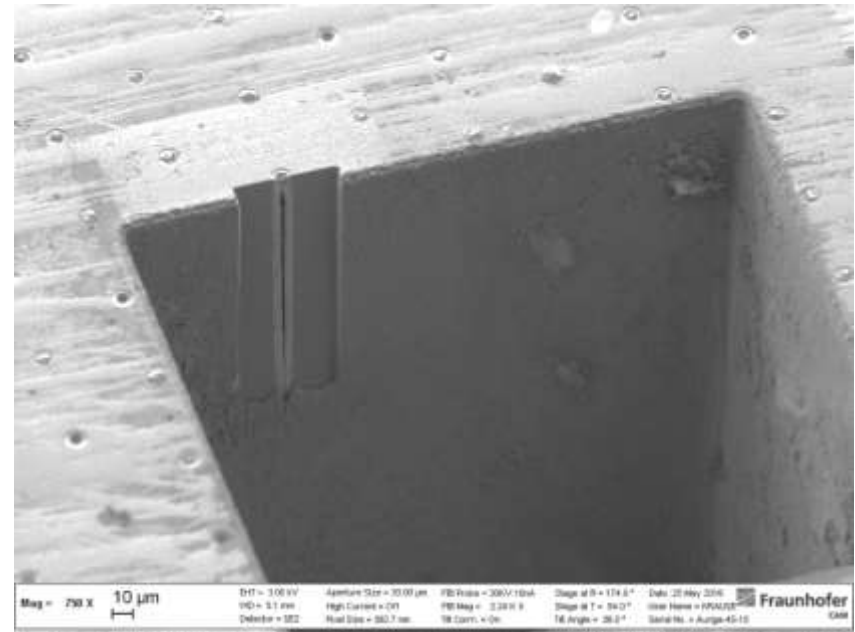
# microPREP™

## Specs

Technical specifications:	
Laser source	DPSS Picosecond Laser Wavelength: 532 nm Max. Power: 3 W
Camera system	FOV: 3.2 x 2.3 mm <sup>2</sup> Resolution: 2.2 μm
Motion system	<u>Rotary axis</u> Stroke: ± 50° Accuracy: < 0,03° <u>Z-Axis</u> Stroke: 1 cm Accuracy: 5 μm
Laser processing	Up to 25mm large structures in <30min Accuracy ± 3 μm



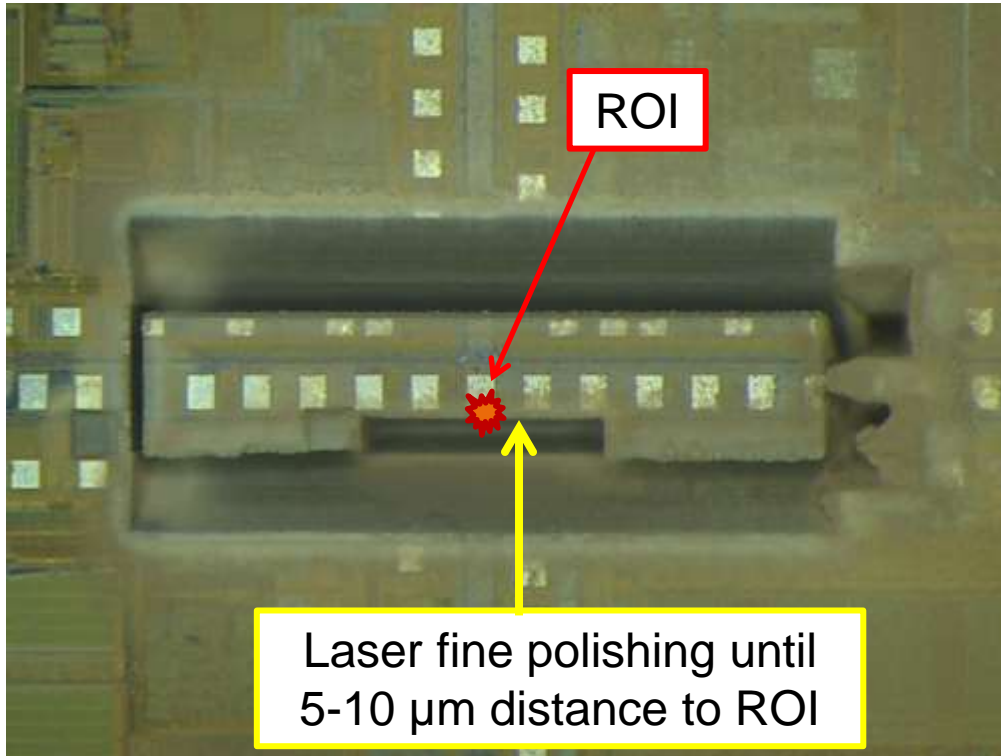
Damage layer <100nm for Si





# Workflow for planar TEM preparation

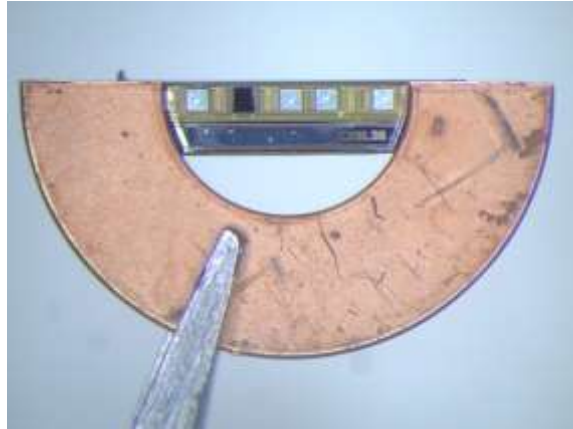
## Laser milling to cut out IC bar



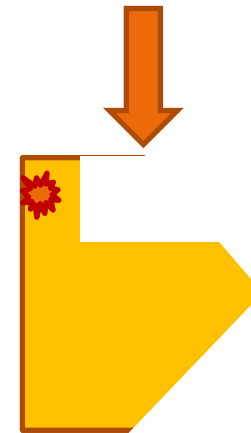
- XL Chunk™ recipe to isolate ROI from rest of IC
- Size of IC bar relative to Cu-ring size :  $2000 \times 400 \mu\text{m}$
- Laser fine polishing to ROI with **5-10  $\mu\text{m}$  distance**
- Short laser preparation time: ~ **6-10min**

# Workflow for planar TEM preparation

## Fixing and final laser milling



Glued chunk

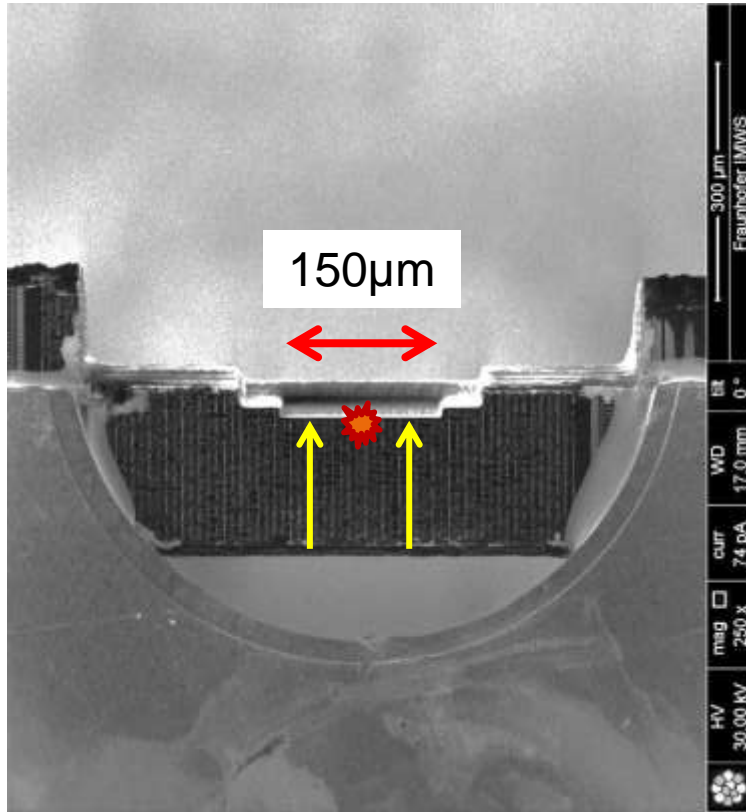


Additional local laser thinning of substrate to reduce FIB preparation time

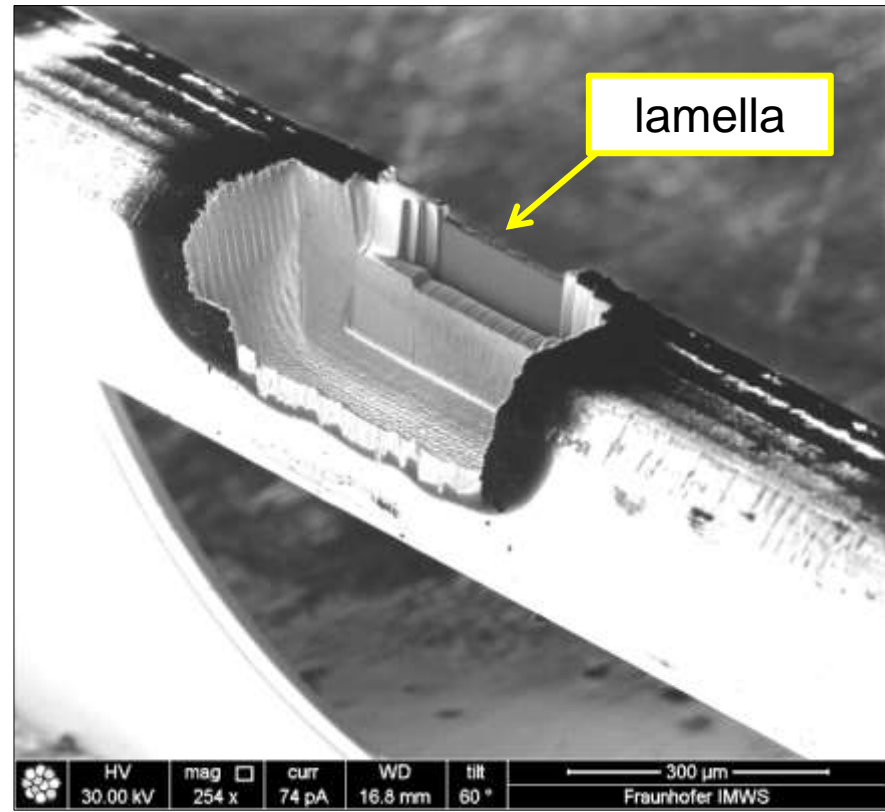


# Workflow for planar TEM preparation

## Plasma-FIB trimming of the lamella



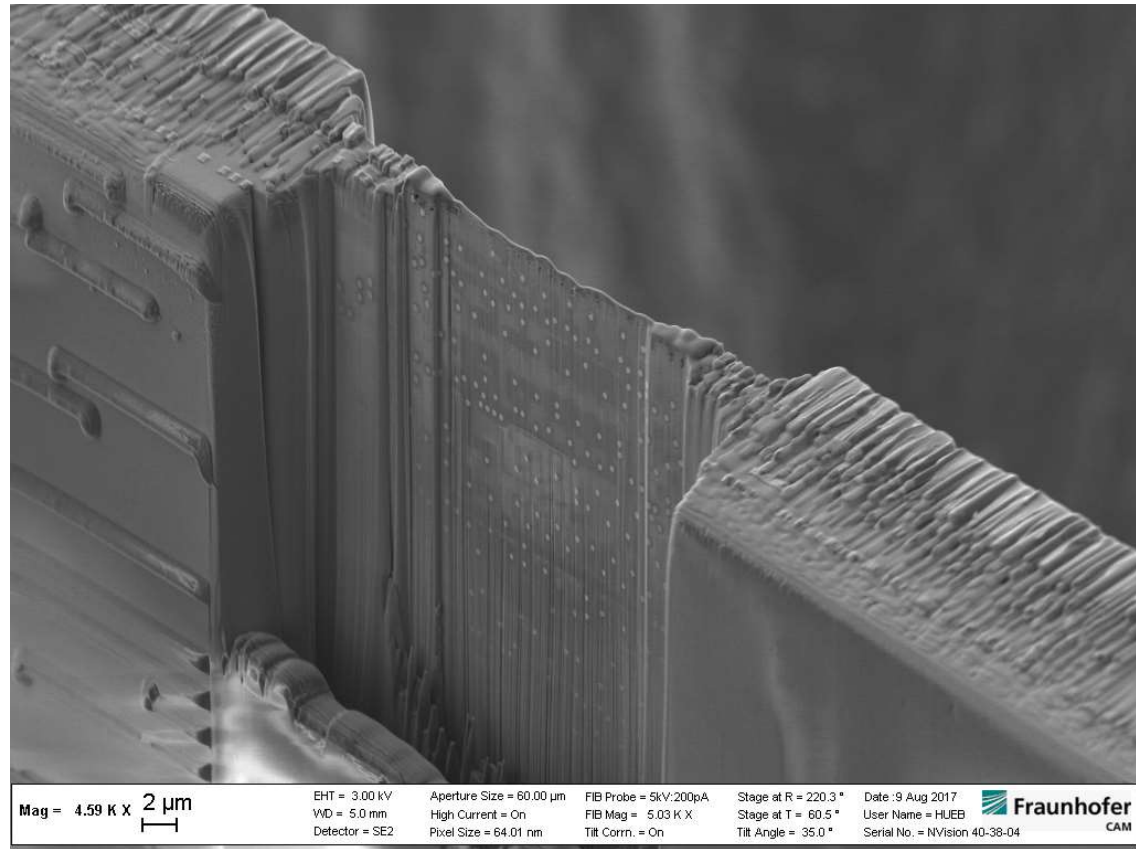
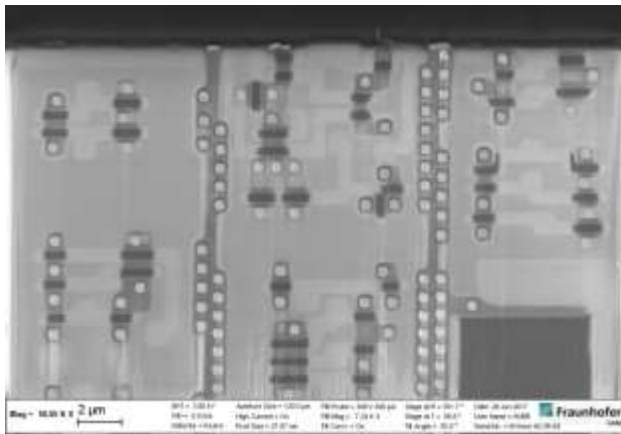
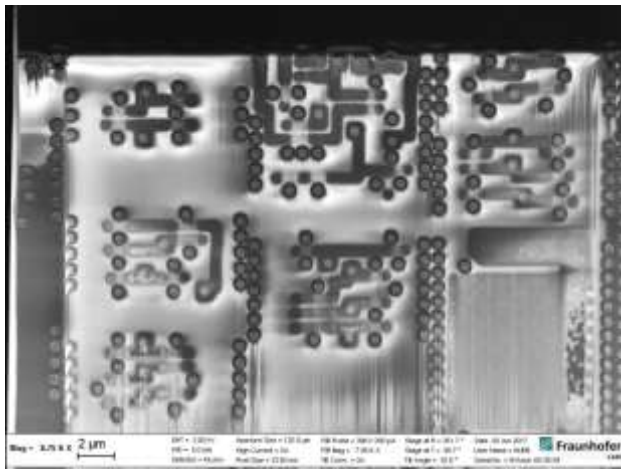
PFIB milling close to ROI



Lamella formation by PFIB

# Workflow for planar TEM preparation

## Final polishing by Ga-FIB

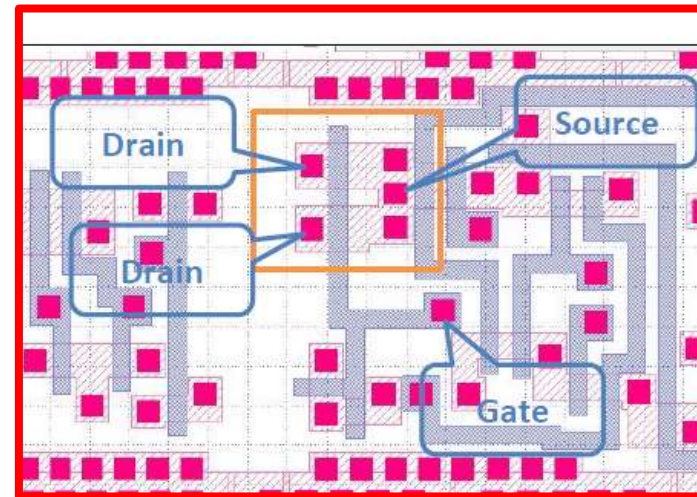
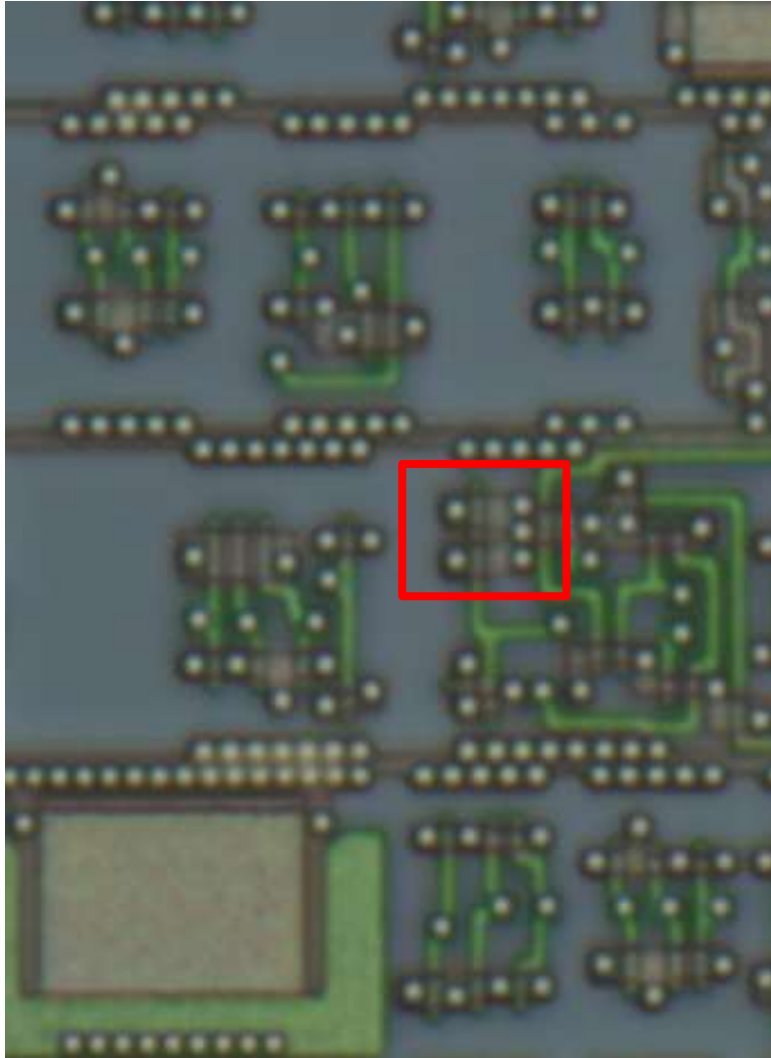


Final TEM lamella

Stepwise removal of metal layers  
in *parallel* to Si substrate

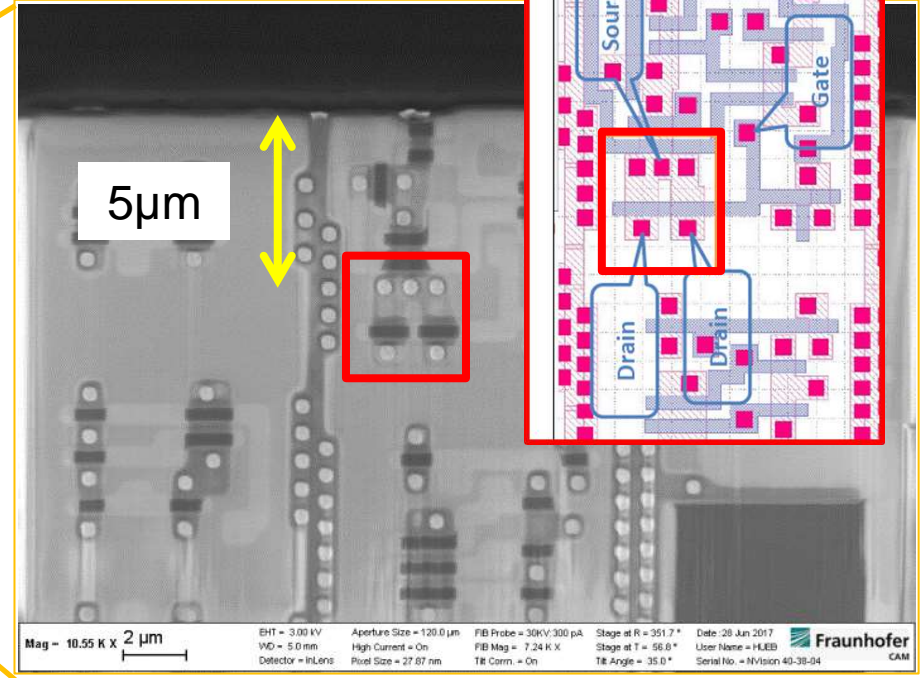
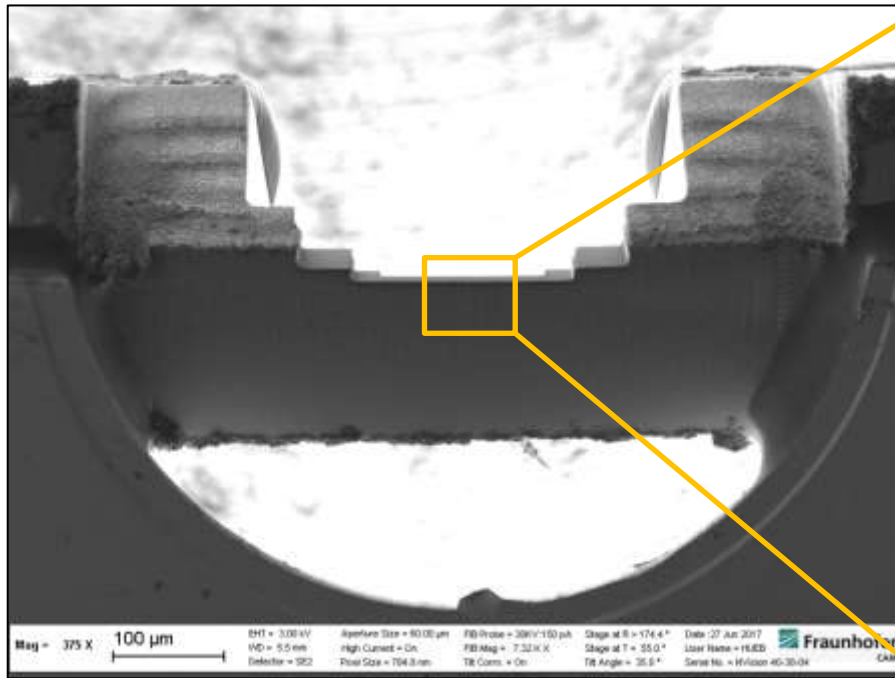


# Case Study at defective IC structure



- Low ohmic PMOS transistor with leakage between source and drain
- Shorts via metal lines could be excluded
- dislocation or other defects in Si-Substrate assumed

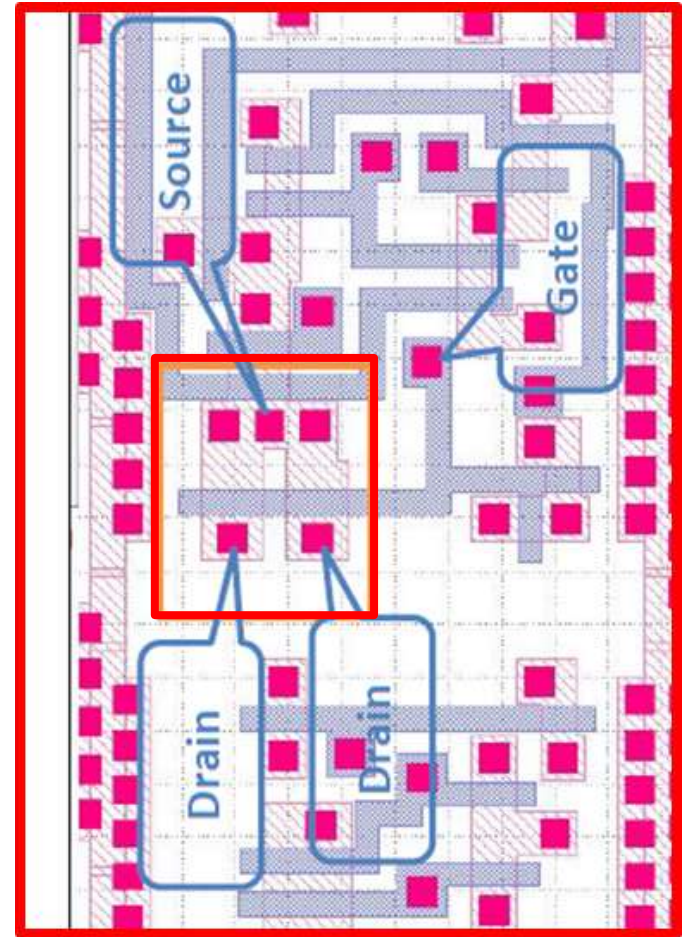
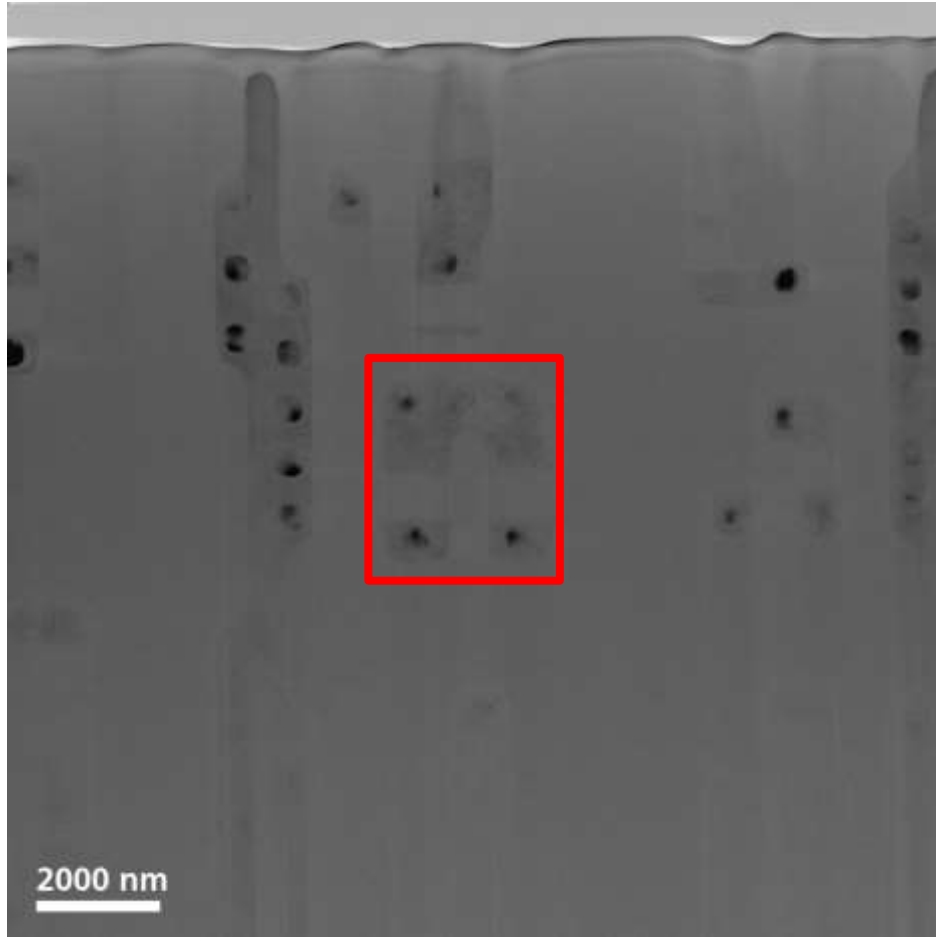
# Case Study at defective IC structure



- Laser milling
- Plasma-FIB trimming
- Ga-FIB polishing

# Case Study at defective IC structure

## Planar TEM investigation

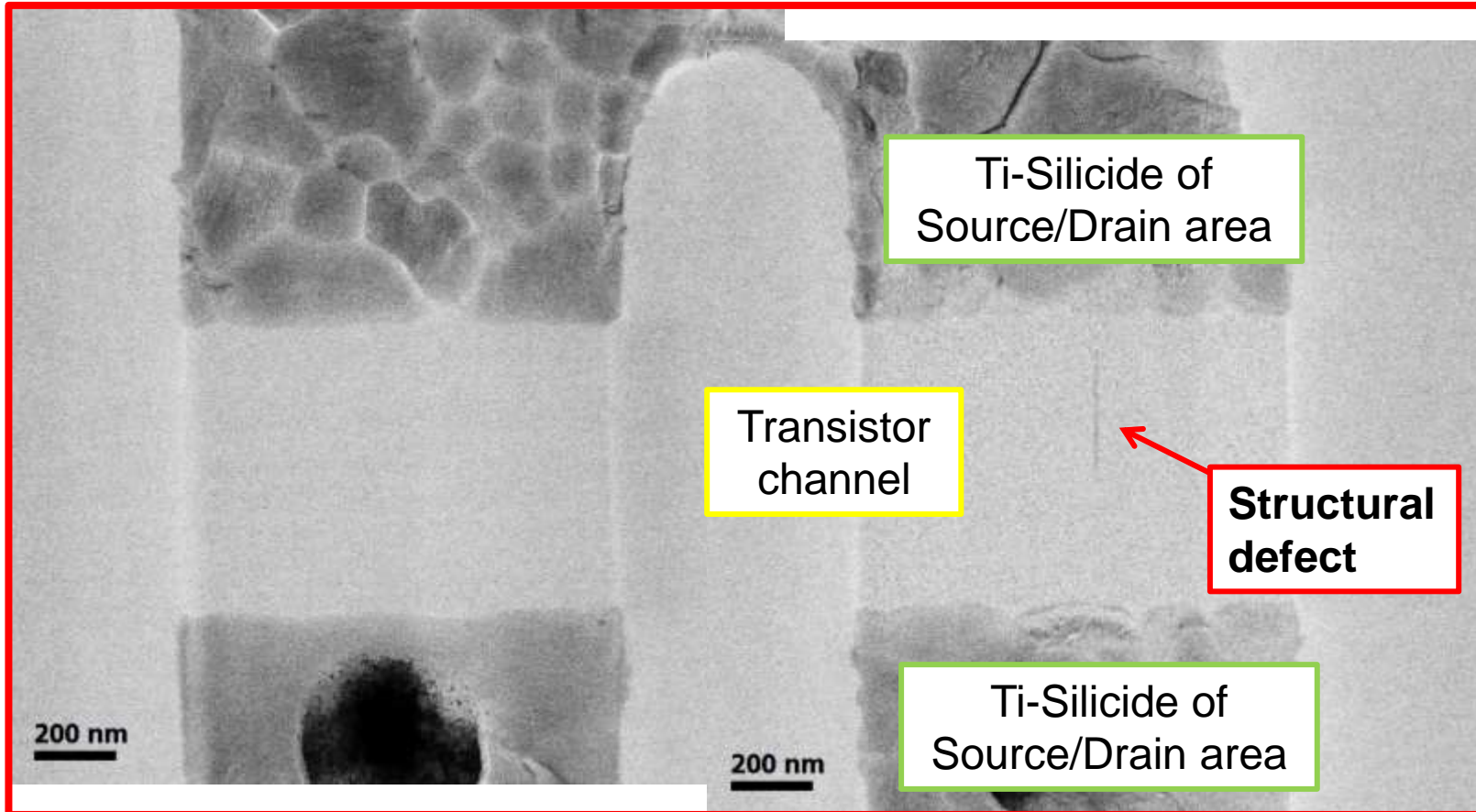


Bright Field TEM image of transistor structure (TEM FEI Titan G2)



# Case Study at defective IC structure

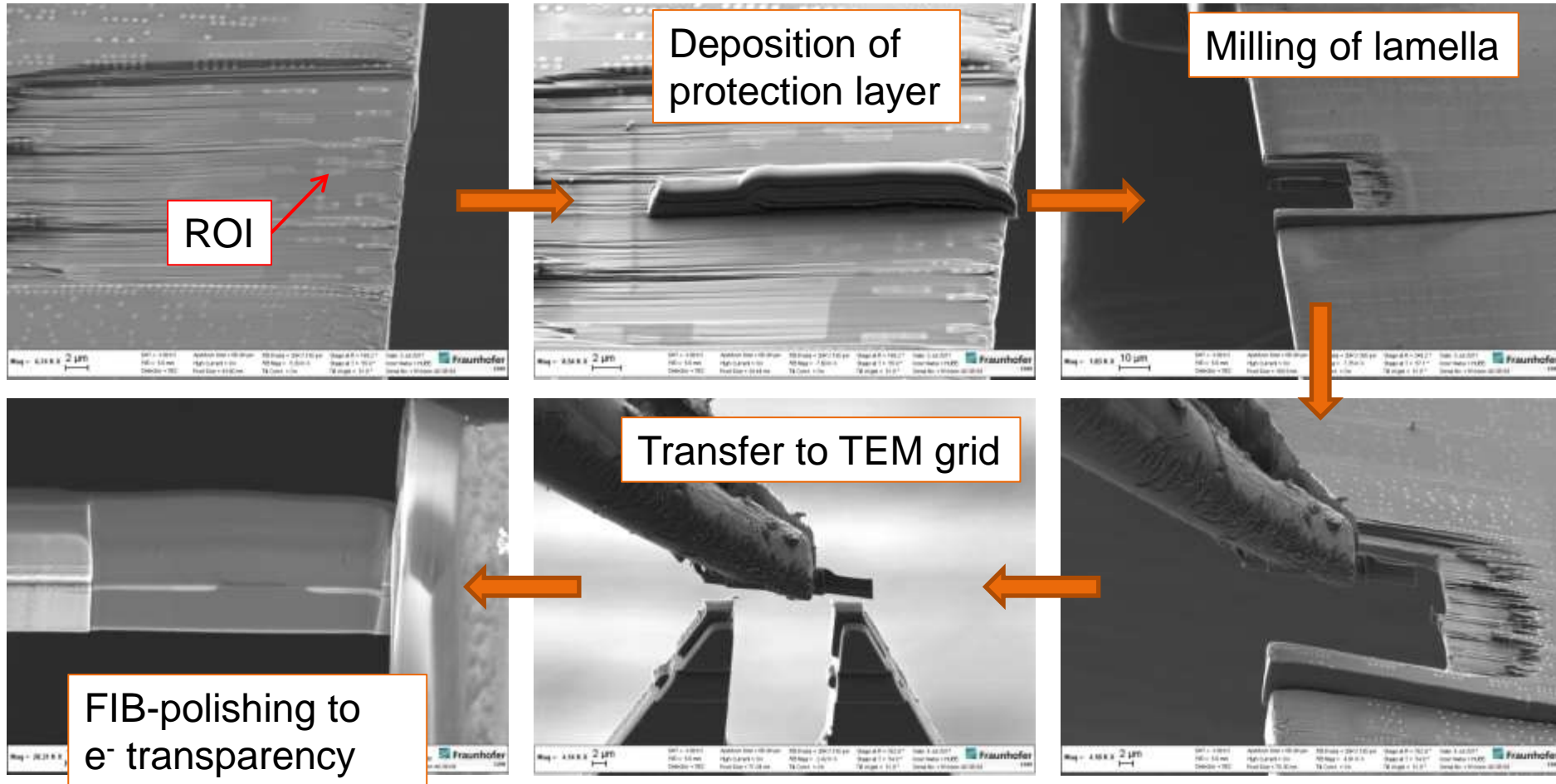
## Planar TEM investigation



Bright Field TEM image of transistor structure (TEM FEI Titan G2)

# Case Study at defective IC structure

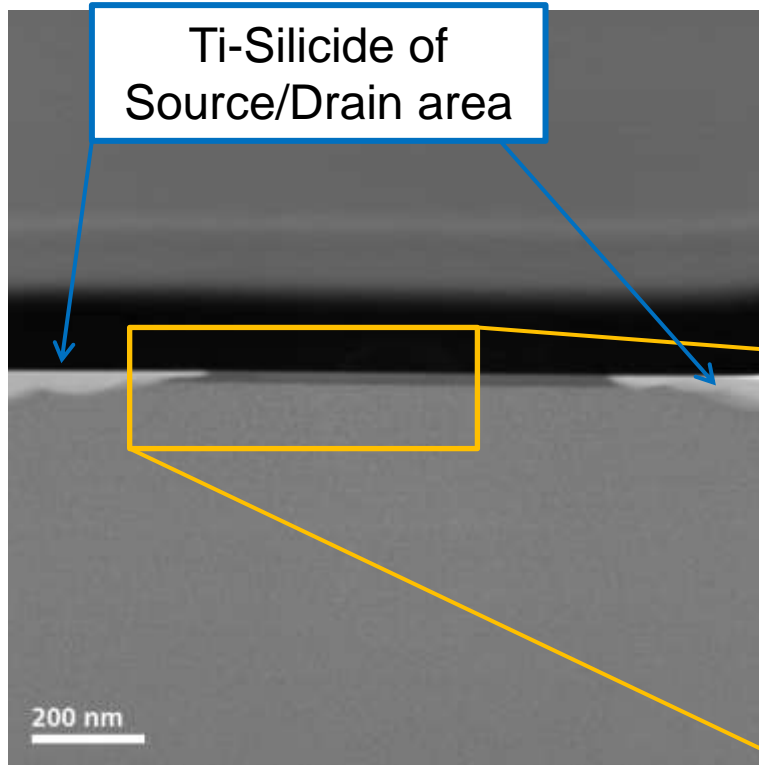
## Preparation of TEM lamella out of planar TEM



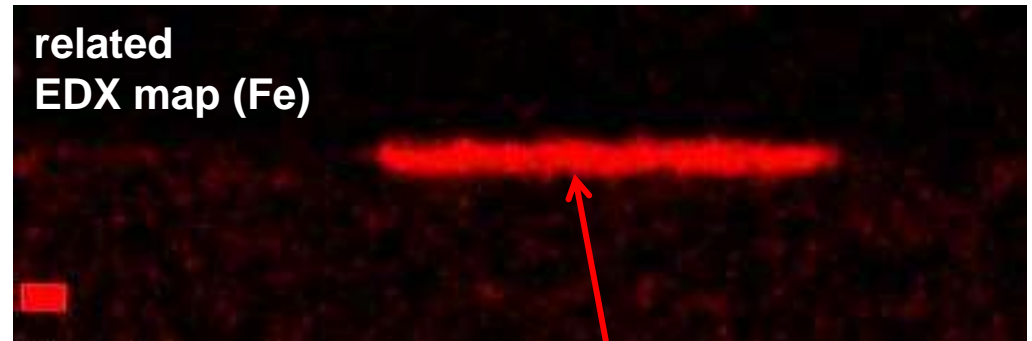
Additional cross sectional TEM for further characterization of the defect

# Case Study at defective IC structure

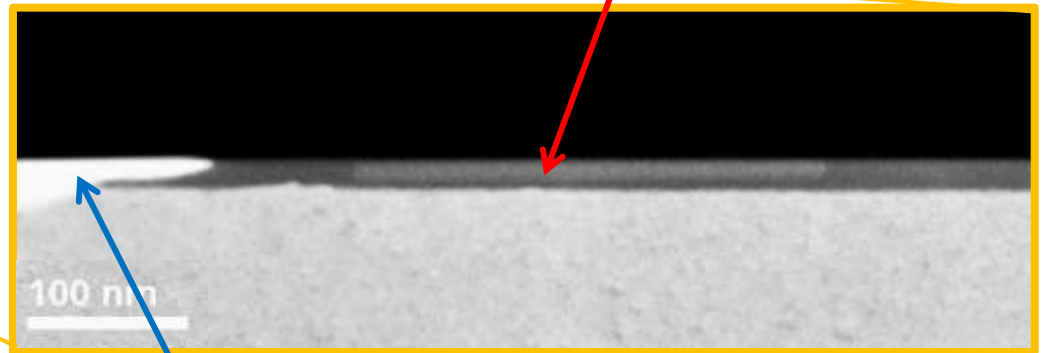
## STEM investigation



HAADF/STEM imaging



Structural defect at channel surface consist of Fe



Ti-Silicide of Source/Drain area



# Summary and Conclusions

- Advanced workflow for fast TEM planar preparation at localized IC defect areas
  - 10min laser milling of IC bar with ROI
  - 5min fixation of chunk on Cu grid
  - 1h further laser and Plasma-FIB trimming -> 150µm lamella
  - About 30min final Ga-FIB polishing of the lamella
- Case study on leaky PMOS transistor channel
  - Linear surface near defect within the channel containing mainly Fe
- Surface amorphisation by FIB delayering of the IC structure → dislocation would be destroyed → additional final milling step by low kV FIB recommended

# Acknowledgement

This work has been performed in the project “SAM3”, where the German partners are funded by the German Bundesministerium für Bildung und Forschung (BMBF) under contract 16ES0348. SAM3 is a joint project running in the European EUREKA EURIPIDES and CATRENE programs.

