# Localised FIB Deprocessing on Advanced Process Technologies

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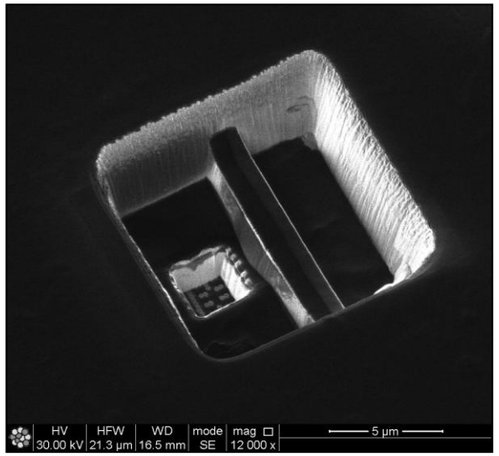
# Background

# What is Deprocessing?

- Deprocessing is the art to remove metal layers uniformly in an IC.

Image source: South Bay Technology

- Can be performed globally, by mechanical polishing, but the FIB offers the possibility to deprocess specific local regions, whilst retaining device functionality



# Why do we Deprocess?

- The requirement to access a particular layer of the device which is sub-surface.

- Once the layer is reached, further failure analysis (voltage contrast, defect analysis, electrical probing, reverse engineering) or circuit modification can be performed to achieve and end result.

# The Mixed Field Problem

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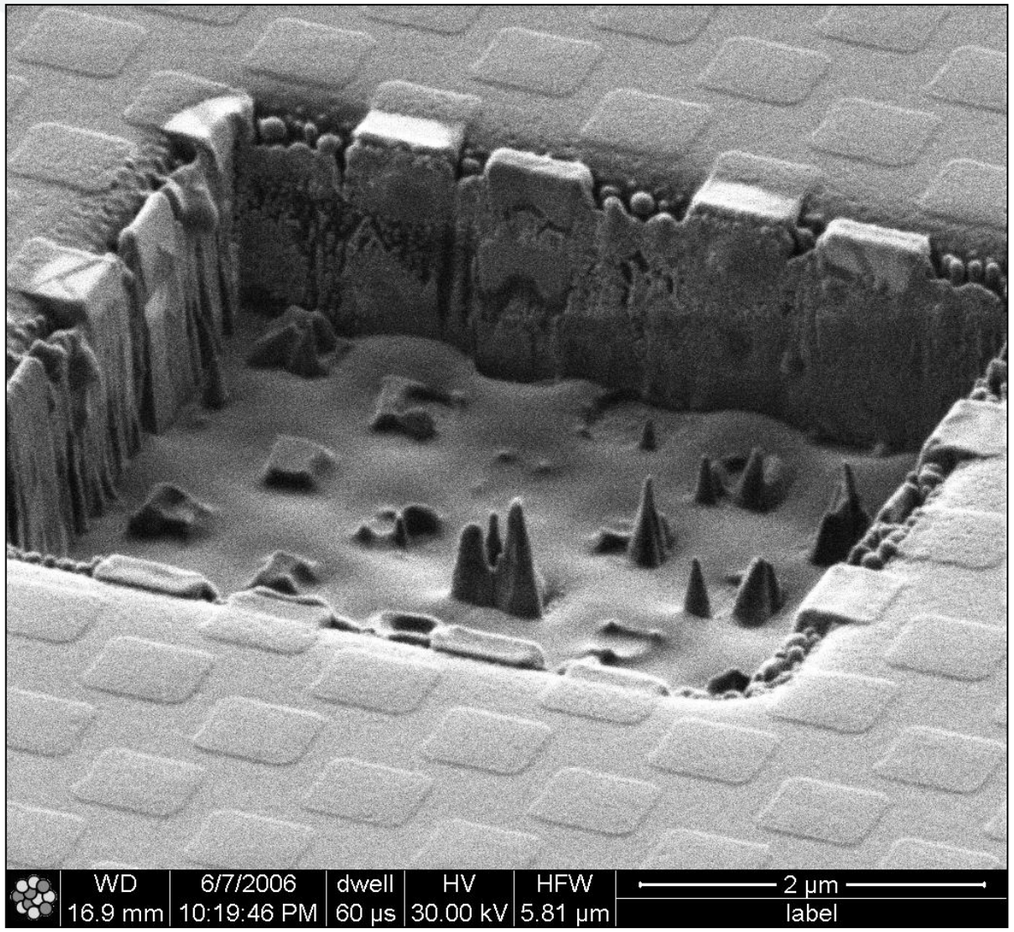
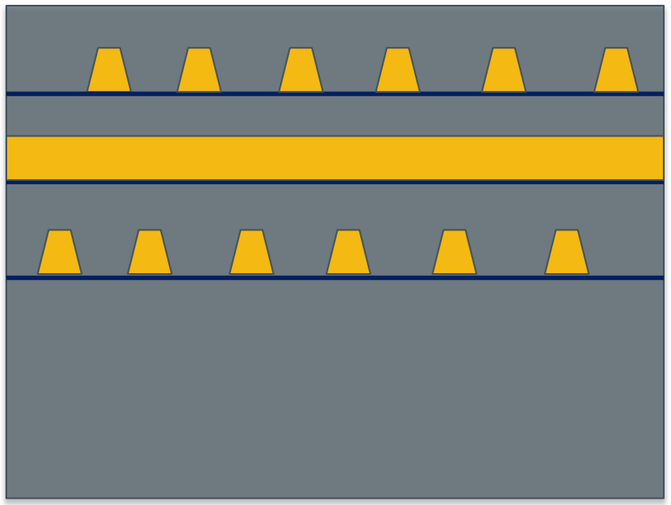



The necessity to evenly mill through different materials with different milling rates introduces a significant challenge. Unpredictable copper grains' orientation makes the problem even more complicated. Gas assisted etching is key for successful de-layering.

# Achieving Planarity



- One option is to use appropriate chemistries and beam parameters to achieve an even etch rate for different materials

# Current Deprocessing Method

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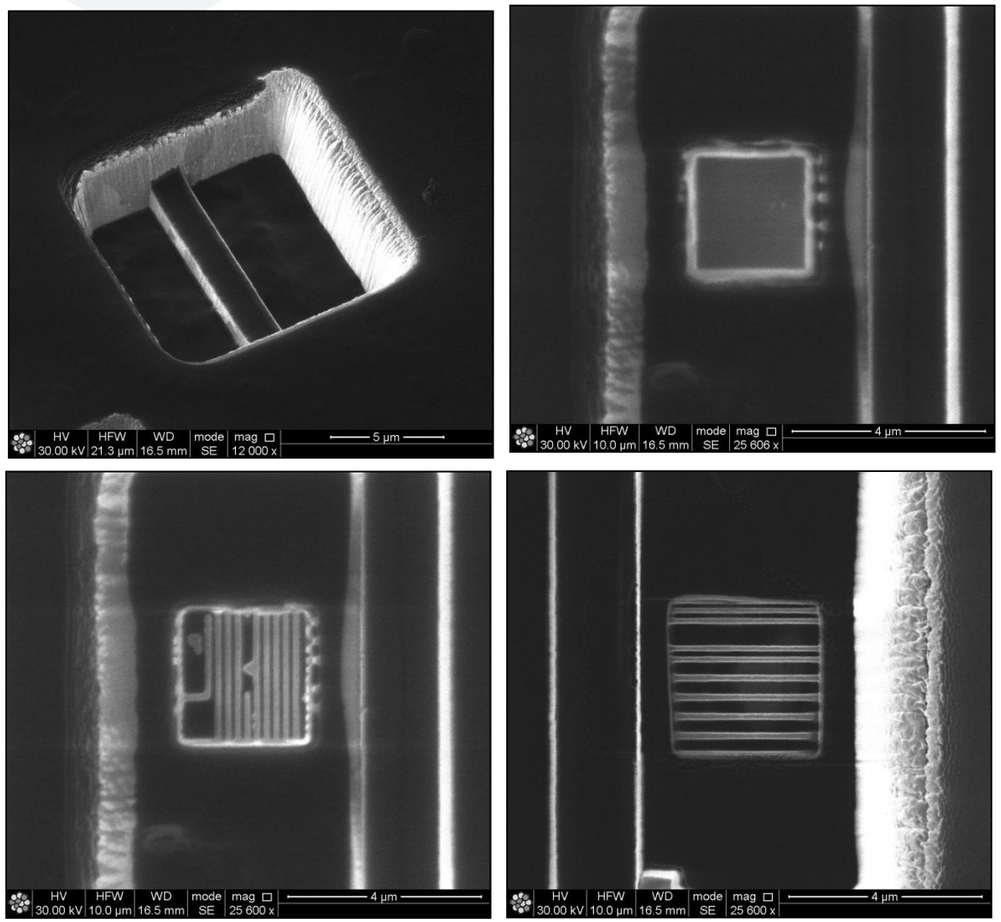
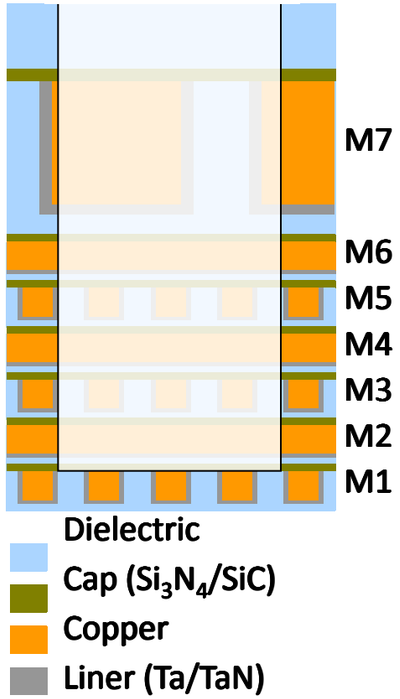
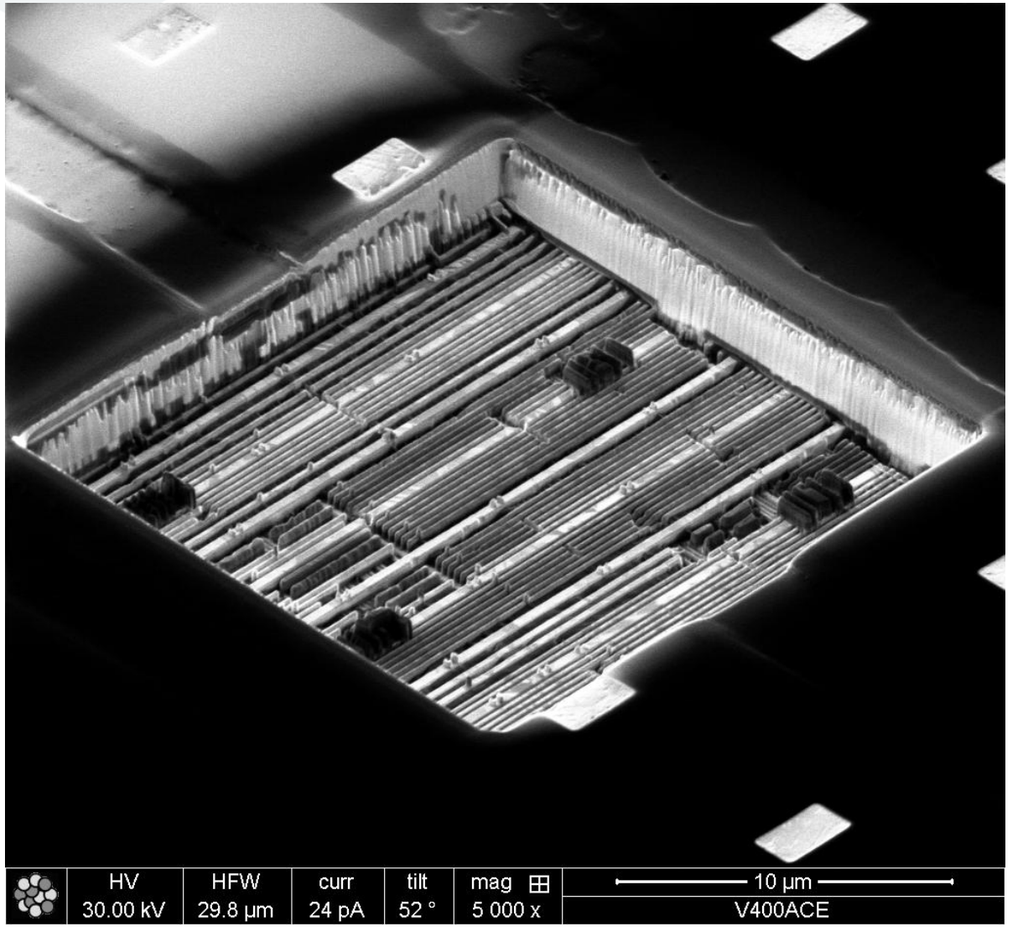



- Alternating of XeF2 assisted etch (for dielectric removal) and H2O assisted etch (for copper removal) is a well known and robust method that is used for “Cu + SiO2” and “Cu + LowK with SiN as an etch stop layer” mixed field planar de-layering. This method is fast and repeatable enough for past backend technologies.

# Current Deprocessing Methods




Although, the “Old Method” provided a good solution for the past backend technologies, one problem was unavoidable. A layer of possibly conductive materials was always deposited on the trench sidewalls as a result of non-volatile materials sputtering.

# The SiC roadblock

# Requirements for Etch Stop Layer in Cu Damascene Processes

- Should have low k
- Be a good copper diffusion barrier
- High etch selectivity properties wrt to ILD
- Compatible with damascene processes

➢ 1st Generation etch stop was SiN

➢ However thick layer is required for etch selectivity

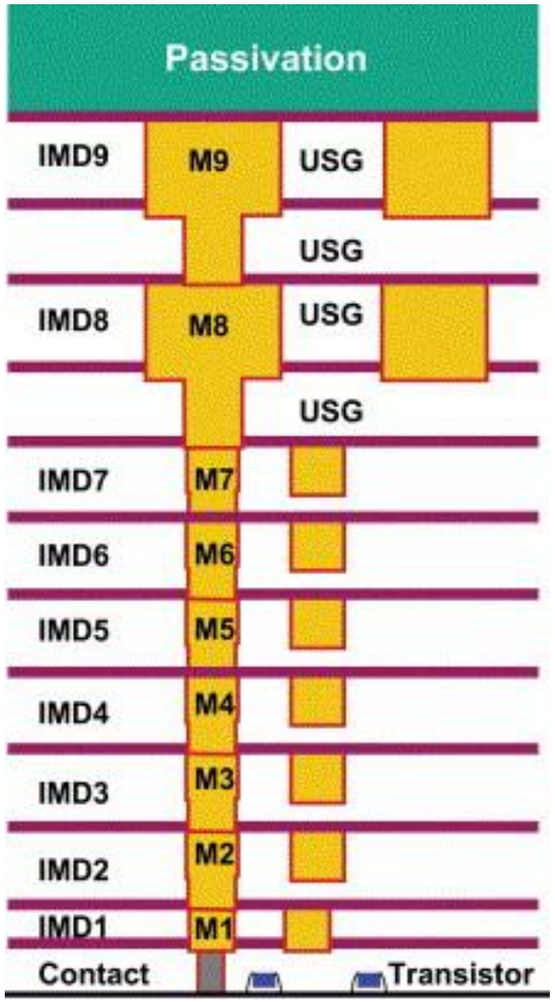
➢ k value was 7.0

➢ Overall k of dielectric stack was impacted

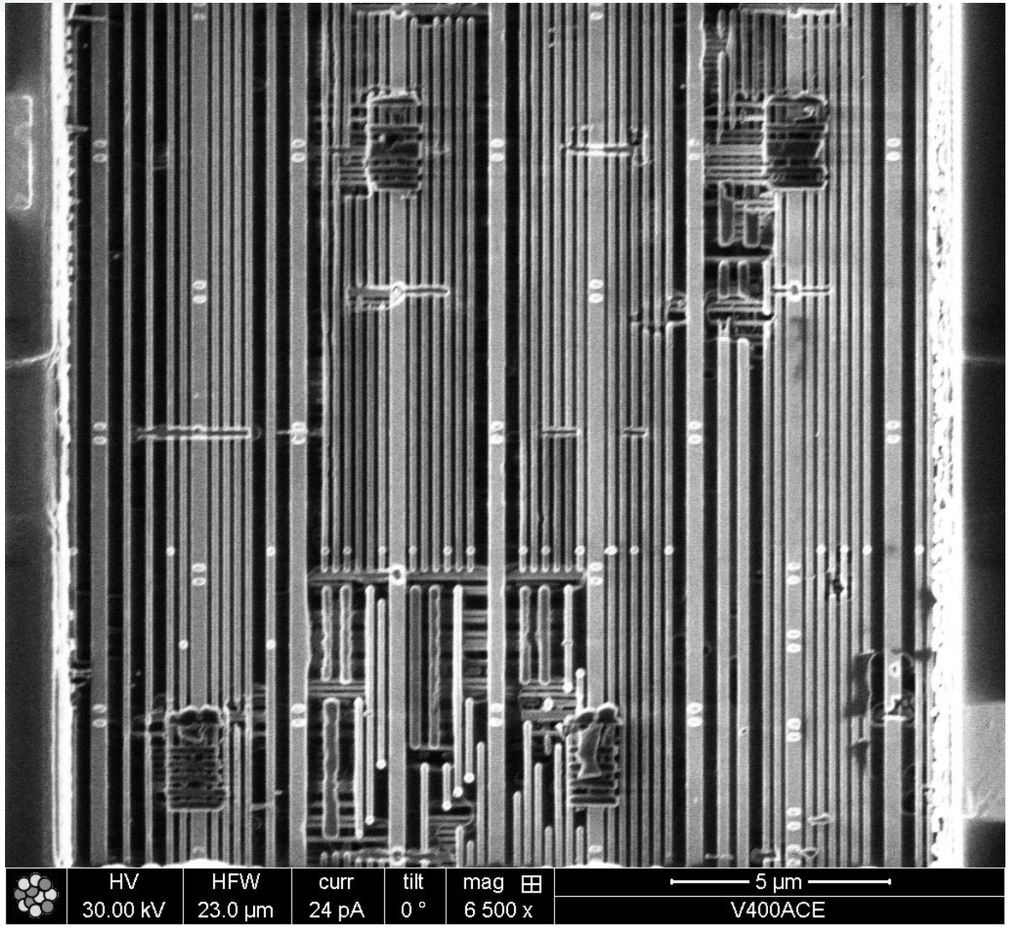
➢ 2nd Generation etch stop is SiC

➢ Better etch selectivity, thinner films possible

➢ k value < 4 possible



# SiC as an Etch Stop Layer




When it comes to “Cu + LowK with SiC as an etch stop layer” combination the “Old Method” is not suitable. H2O creates highly volatile compounds (COx) with carbon and therefore cannot be used for selective copper removal anymore.

The attempt to apply this method to “Cu + LowK with SiC as an etch stop layer” combination leads to uncontrollable etch of dielectric.

# Planar Deprocessing with New Chemistry

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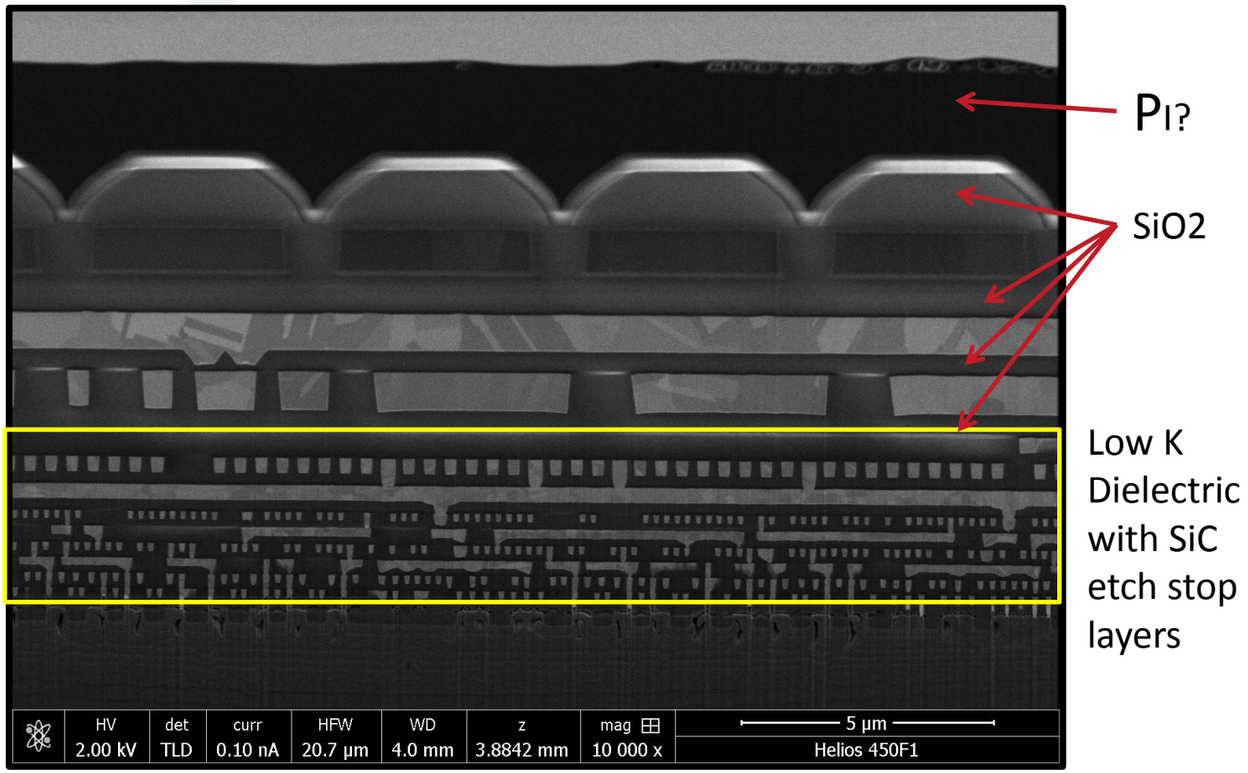
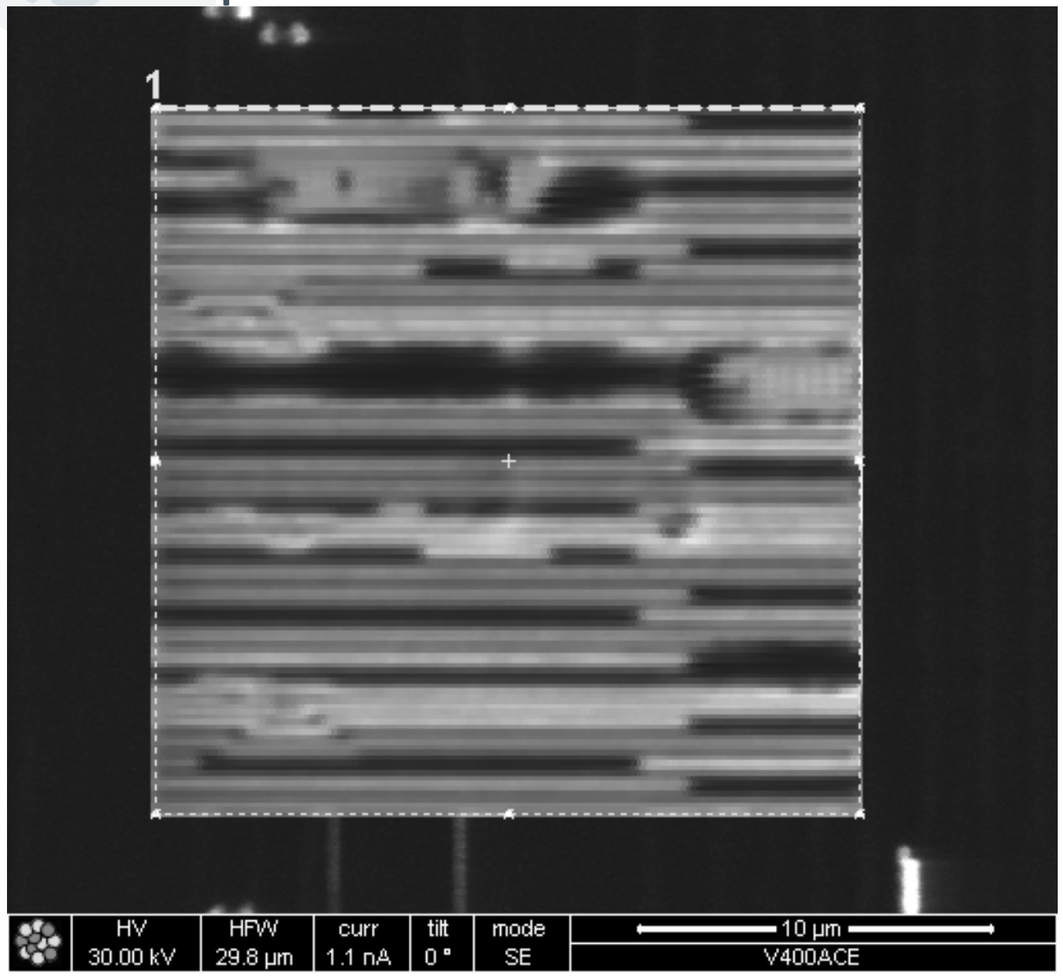
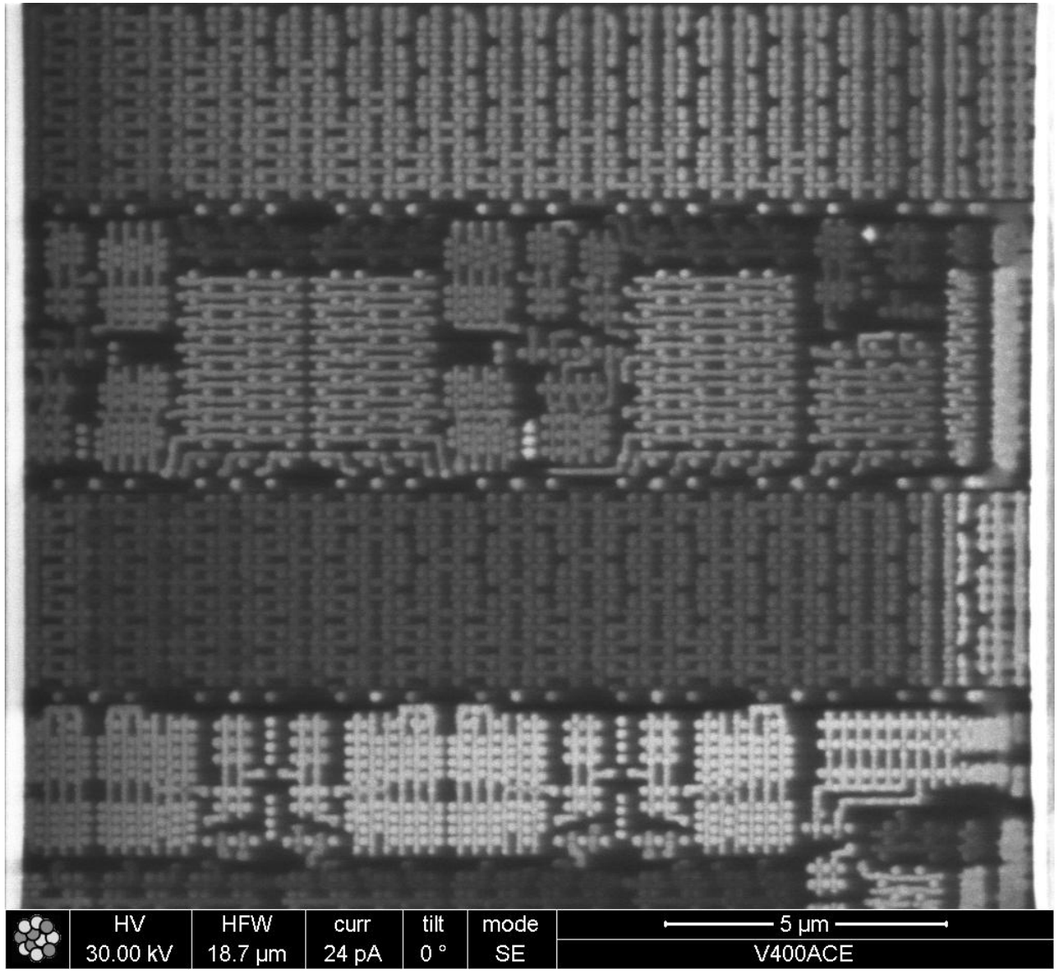



- Excellent planar deprocessing has been achieved on Cu-low k regions using new FEI chemistry
- None of the problems associated with $XeF_2/H_2O$ and SiC are observed with clean removal of the SiC layer
- The process is slower than previously allowing the user more control over the deprocessing

# Planar Deprocessing Results

## 28 nm process

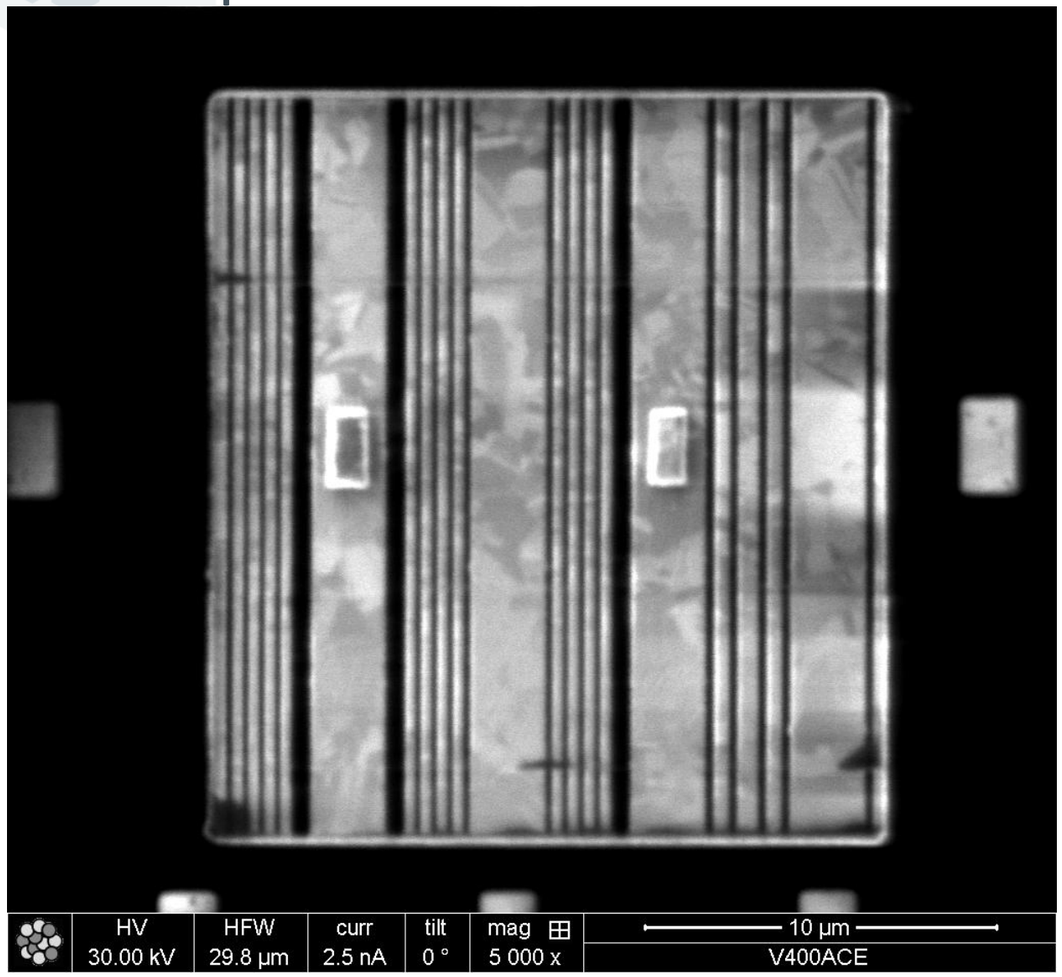


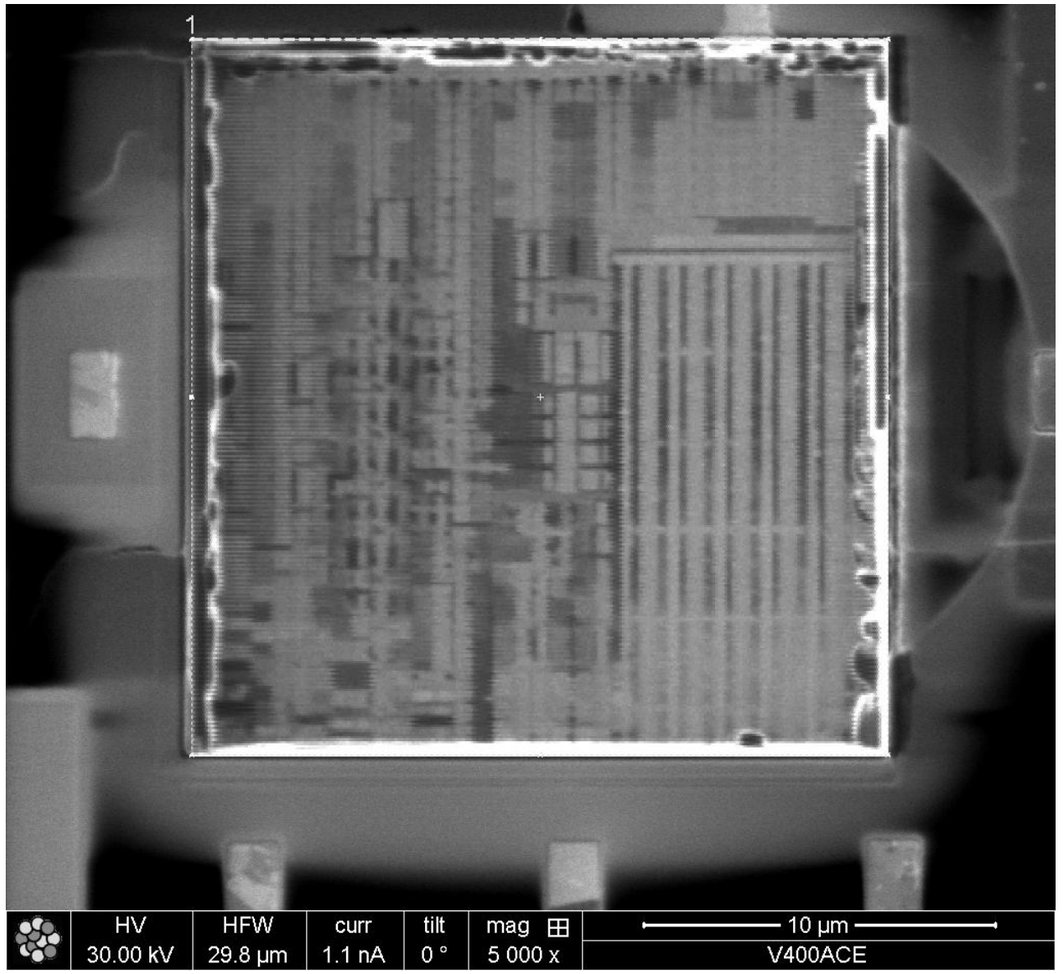




20 µm x 20 µm area delayered uniformly from M9 down to exposure of poly-silicon

# Planar Deprocessing Results

## 22 nm process

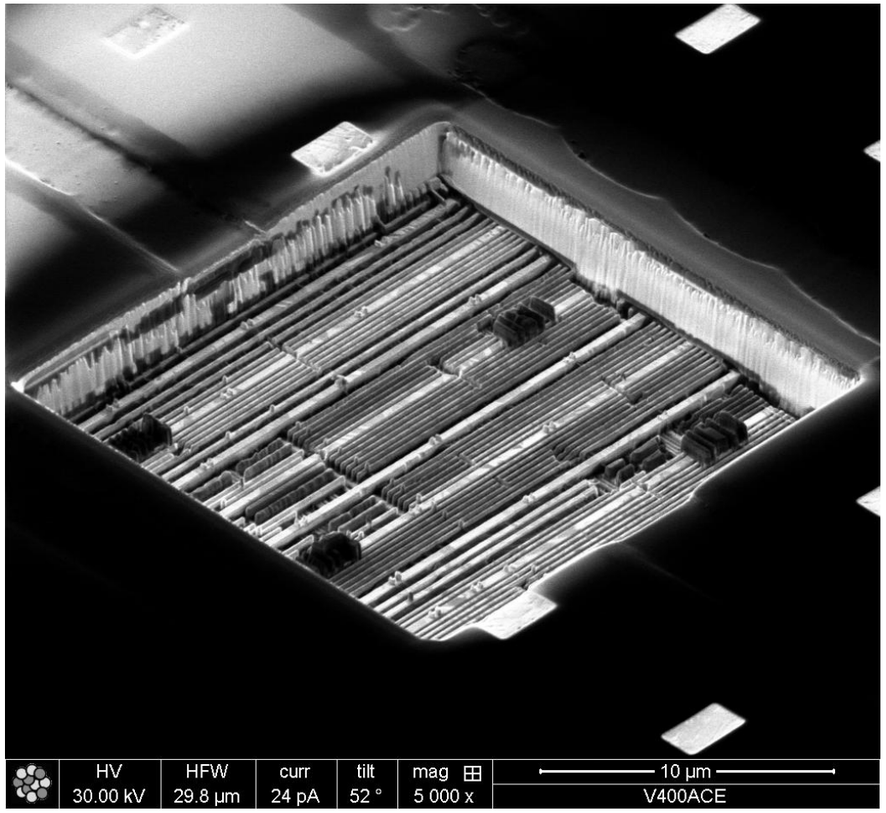


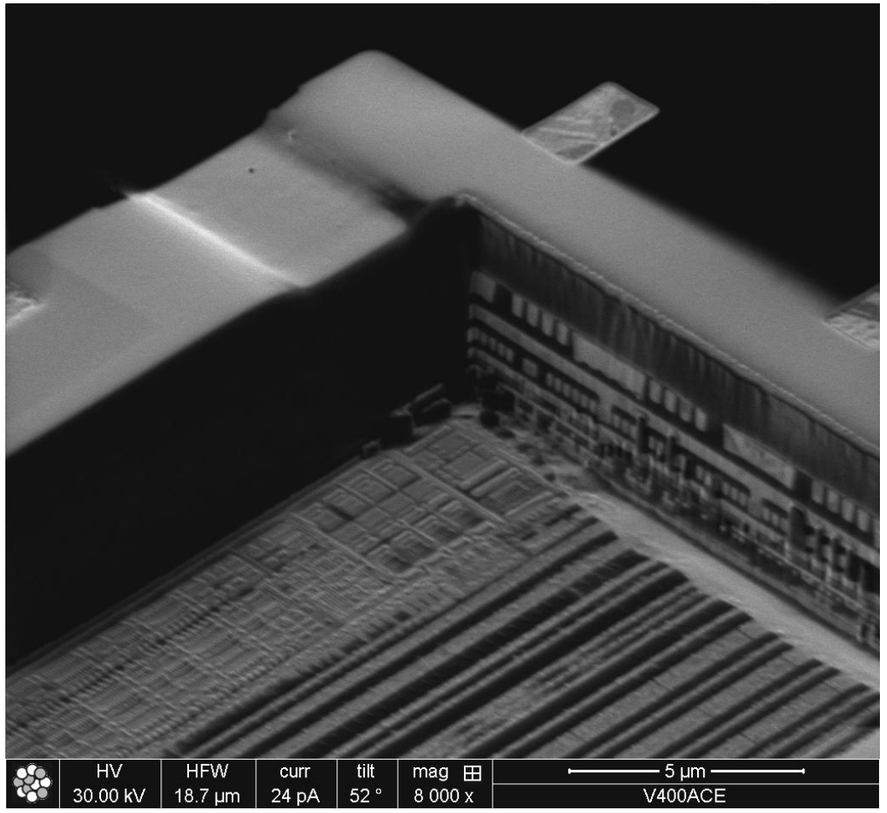

20 µm x 20 µm area delayered uniformly down to M1

# Planar Deprocessing Results

## Reduced Redeposition using new chemistry




$XeF_2/H_2O$ conventional delayering




New Chemistry delayering

# Conclusions and Future Work

- Deprocessing/delaying is an important technique in failure analysis labs for various applications.
- Today's aggressive technologies make it difficult to use existing methods to retain delayering planarity
- New Chemistry works extremely well for deprocessing/delayering in advanced process technologies which use SiC as an etch stop layer
- Is available in GIS format for single beam FIB and SDB systems
- Customer specific recipes provided by FEI
- Further chemistry work is underway to include delayering of Cu/$SiO_2$ regions with a single gas chemistry and a further reduction of redeposition

# Thank You