credence

Issues to Be Address for Improved Circuit Edit Productivity

TR Lundquist, T Malik, R Jain, D Renard, VV Makarov

European FIB User Group, 8 Oct 2007, Arcachon, France

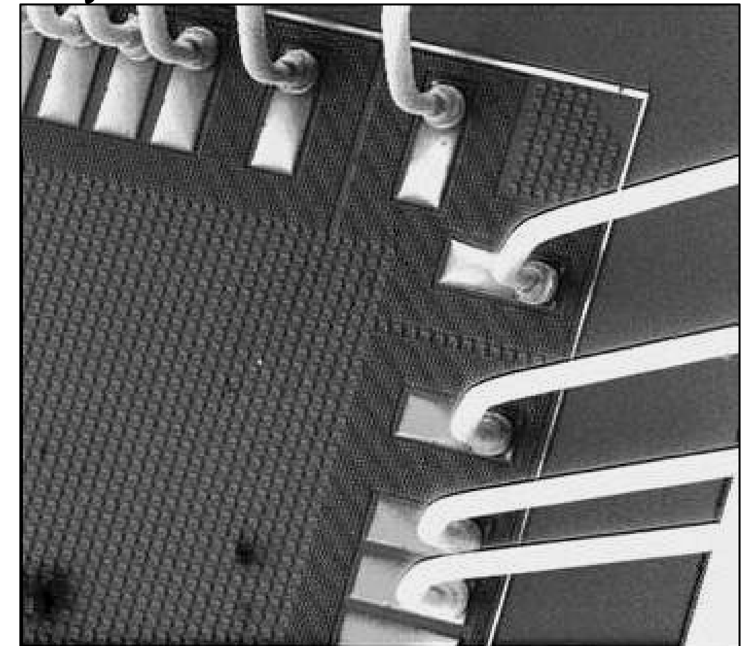
What the Circuit Edit Issues are:

- Top Aluminum metallization
- Blind navigation
- Copper metallizations
- Low-k dielectric
- Conductor overspray clean-up
- Impossible edits
-

- There may be more but these are what will be reviewed along with posssible solutions

Top Al Metallizations

- Top Al used for optimized gold wire bonding (thick Al)
  - **For fab process uniformity Al dummy fill density is "uniform"**
  - **Al dummies add topography**
- Edits must be done under these top level dummies
  - **Working around these is clumsy & time consuming**
- Solution presented in EFUG 2007 Poster by M Nobile et al.
  - **See this for more information**



Blind Navigation

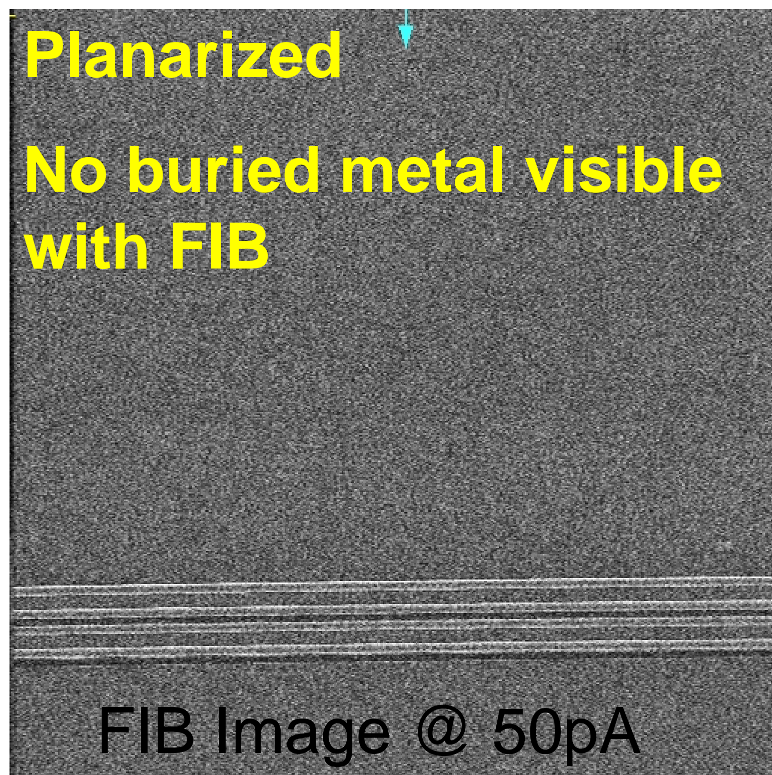
- Because of CMP, few features visible in FIB
- Stage accuracy helps greatly
- But are we sure when we can’t see
  - An error is too costly
  - So pilot holes are made to confirm position
  - Time is consumed

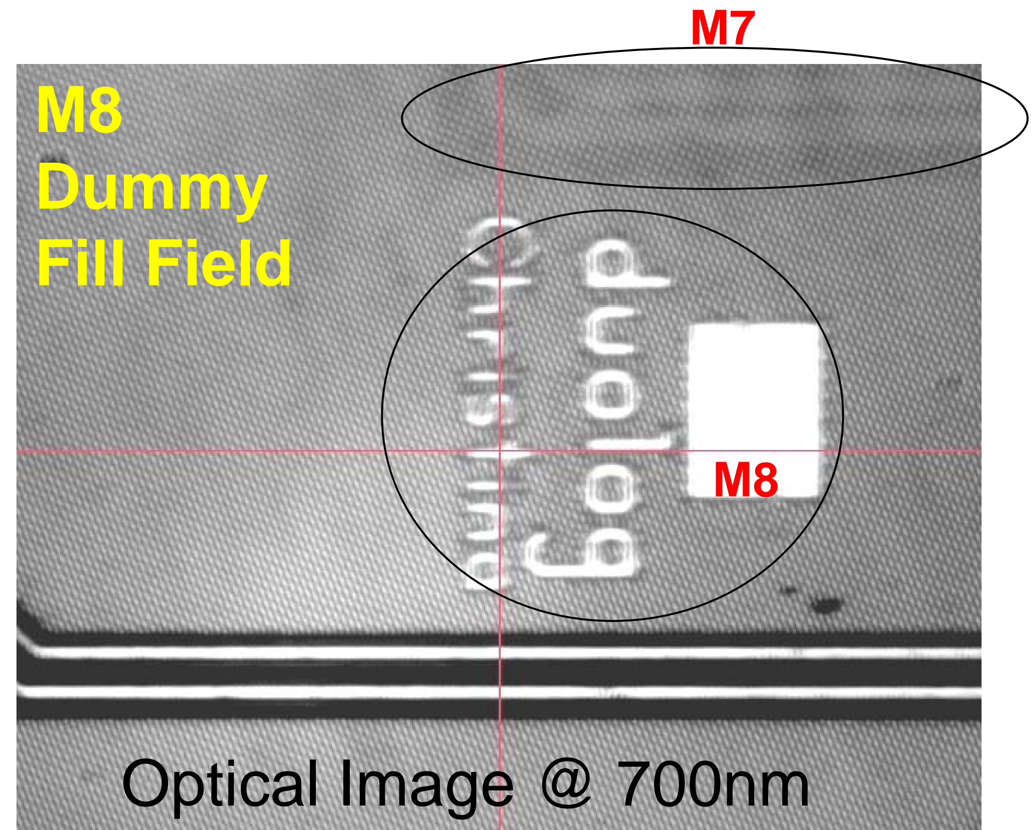
credence

Blind Navigation

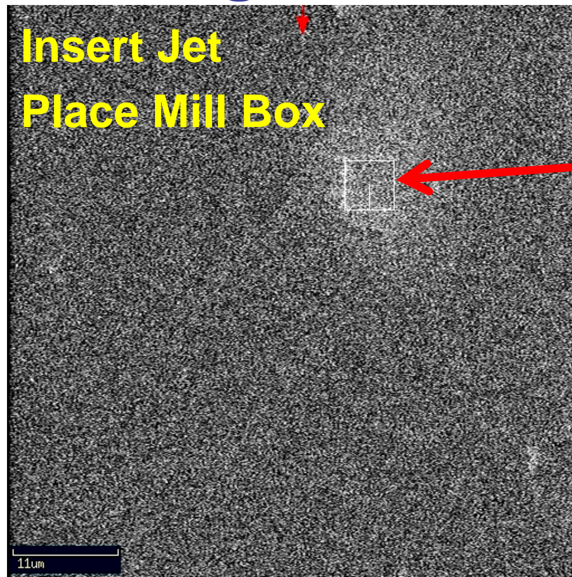
With light you are not blind

- **You can "see" through dummy fill**
- **With light, alignment can be made to CAD**

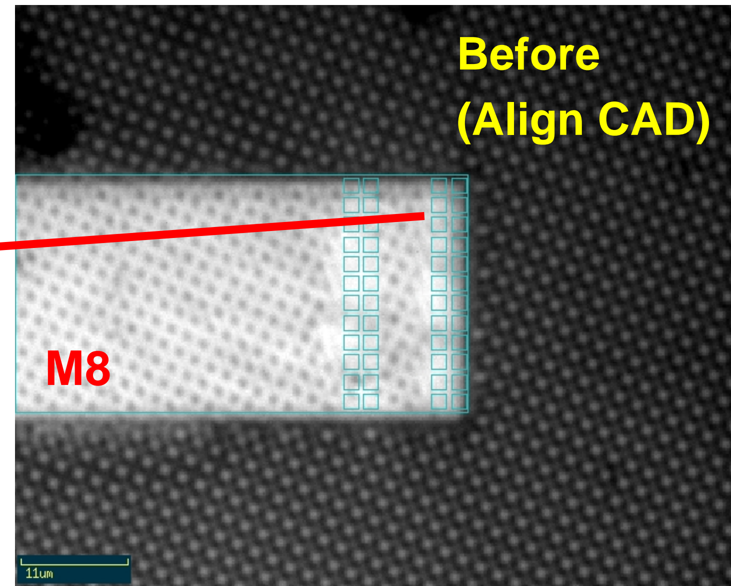




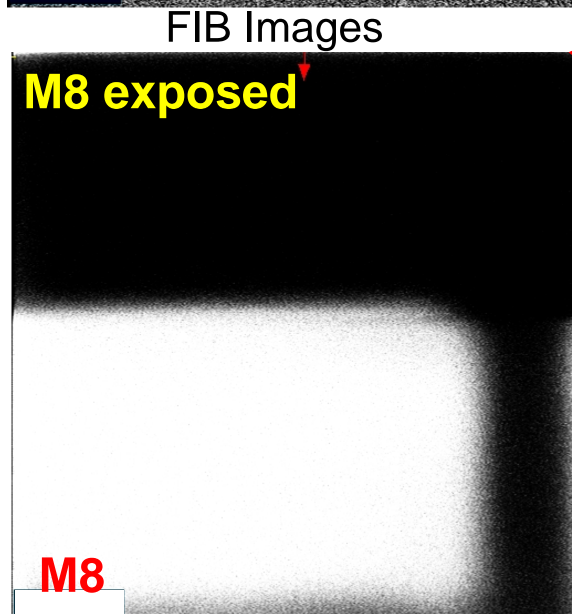
Blind Navigation Example

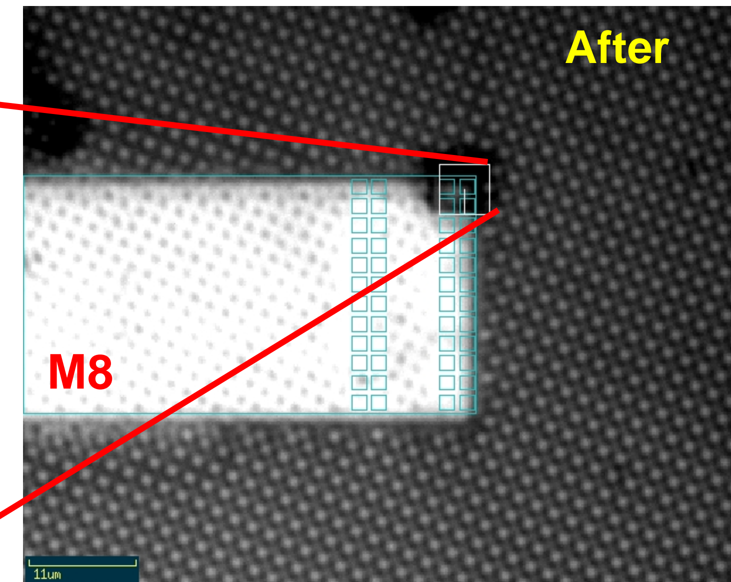


FIB Images



Optical Images





Copper metallizations

- **Copper unlike Al has smaller grains**
  - These grains etch at different rates depending on grain orientation relative to ion beam
- **Heavy halogens are the answer for Al**
  - Heavy halogens are I, Br, Cl
  - Heavy halogens corrode copper
- **Solution: not accelerate removal of Cu but decelerate removal of SiO_2**
  - Protect the dielectric
  - Process is slower
  - H_2O has been used since at least 1998
  - Oxidizing Cu makes it non-conductive
  - Oxidizing SiO_2 makes it more sputter resistant

Expose M1 (7 x 7um area) through Cu bus

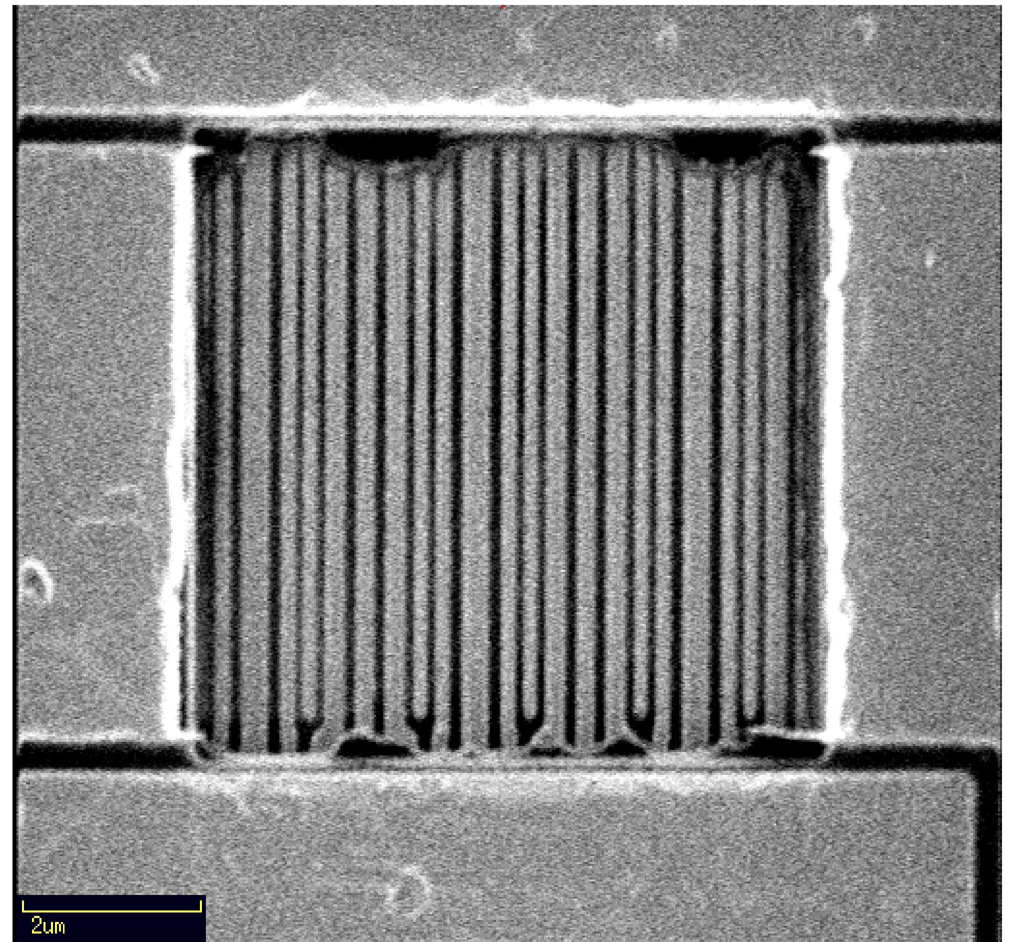
credence

Results:

1. **Power plane etched through**
   - Clean cut—all Cu grains removed
   - Dielectric under cut whole—completely intact
   - Dielectric under cut was flat

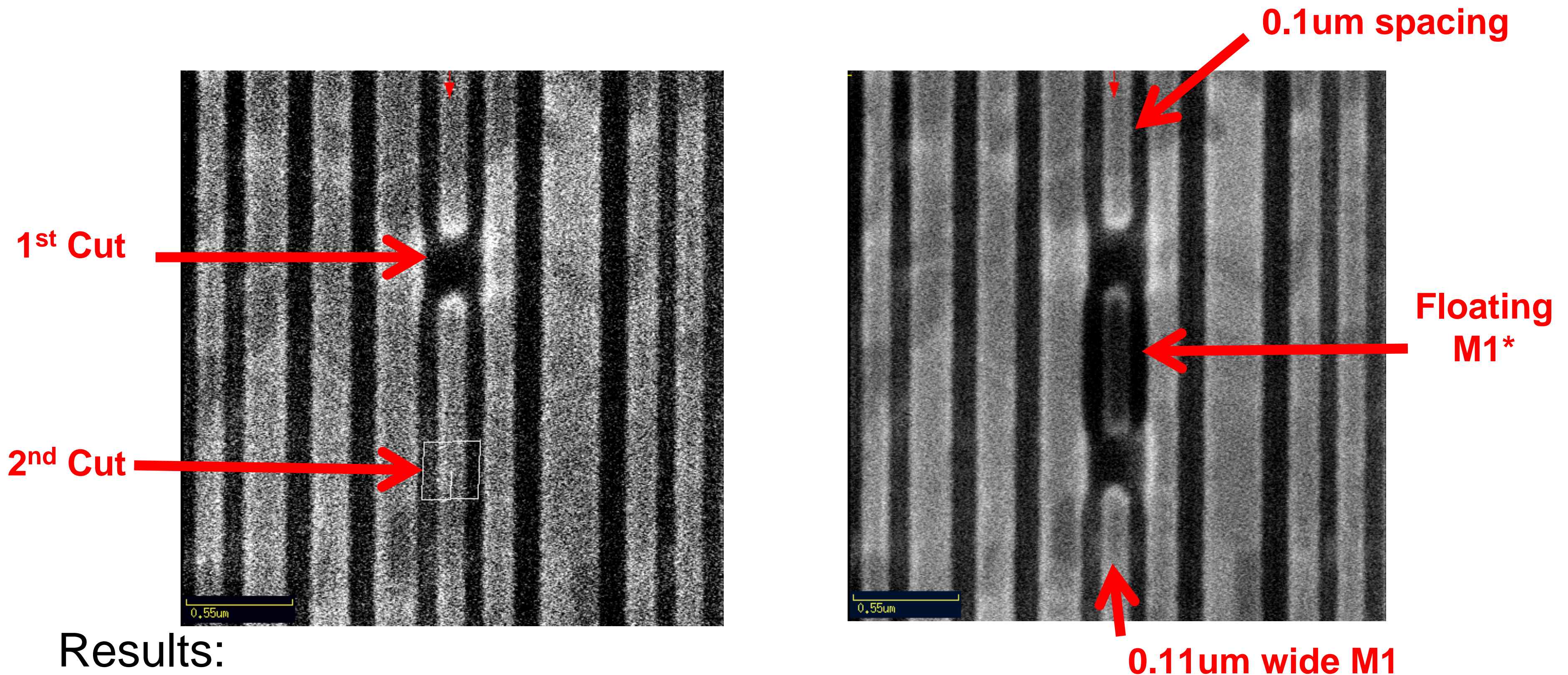
2. **M1's evenly exposed**
   - Underlying dielectric protected
   - All Cu traces intact
   - All Cu traces isolated

3. **Working in a large area improves success rates**



Isolate narrow-dense M1 trace by cutting 2x

credence



Results:

M1 cut at two places using CU2 chemistry

Small M1 trace isolated* when 2nd cut completed

No Cu re-deposition in or around edit area

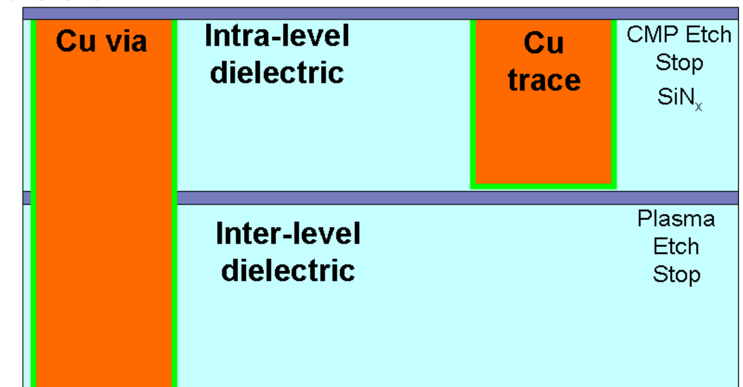
No dielectric over-etch under cut areas

Adjacent Cu traces remain unscathed

- **Low-k dielectric in advanced ICs**
  - C substituted for Si; the less Si the lower the k
  - SiN_x, SiC, etc higher k dielectrics act as process etch stops
  - Etch stops are being eliminated

SiO_2 → CDO

- **Low-k enables thinner dielectrics**
  - Good news as stack height is less
  - Bad news margin for error is greatly reduced
    - Not a low-k issue so much as Cu above
    - Low-k is issue when in Cu planes
    - Slower process

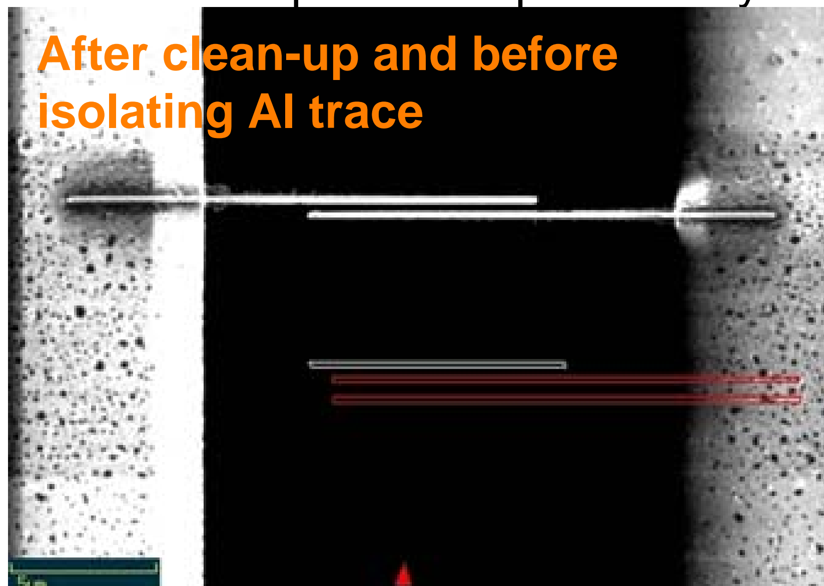


- **Low-k is more delicate than SiO_2**
  - Most recipes for SiO_2 do not work for low-k
    - Low-k etch stops makes old recipes look like they are working
  - Goal is for low-k to be air gaps—k = 1

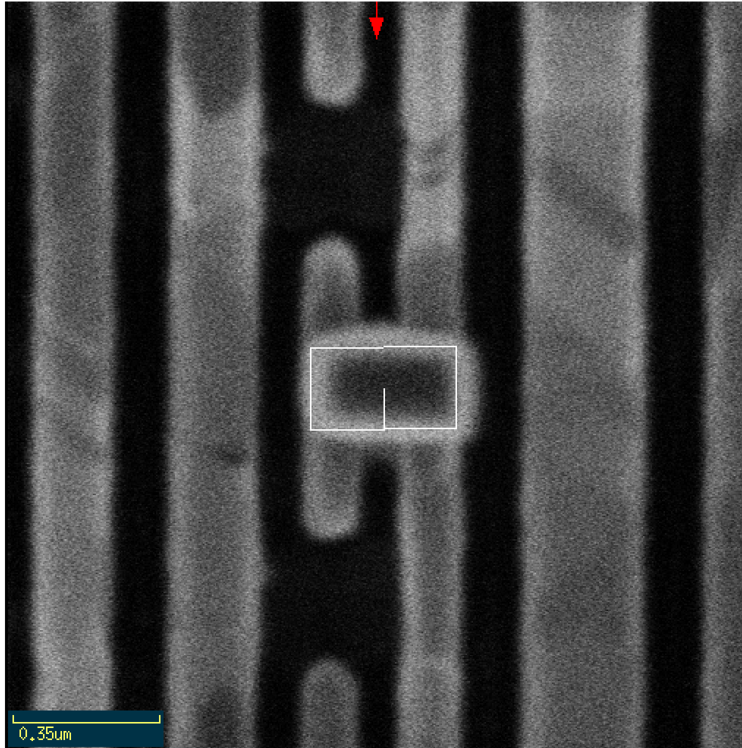
Conductor Overspray Clean-up

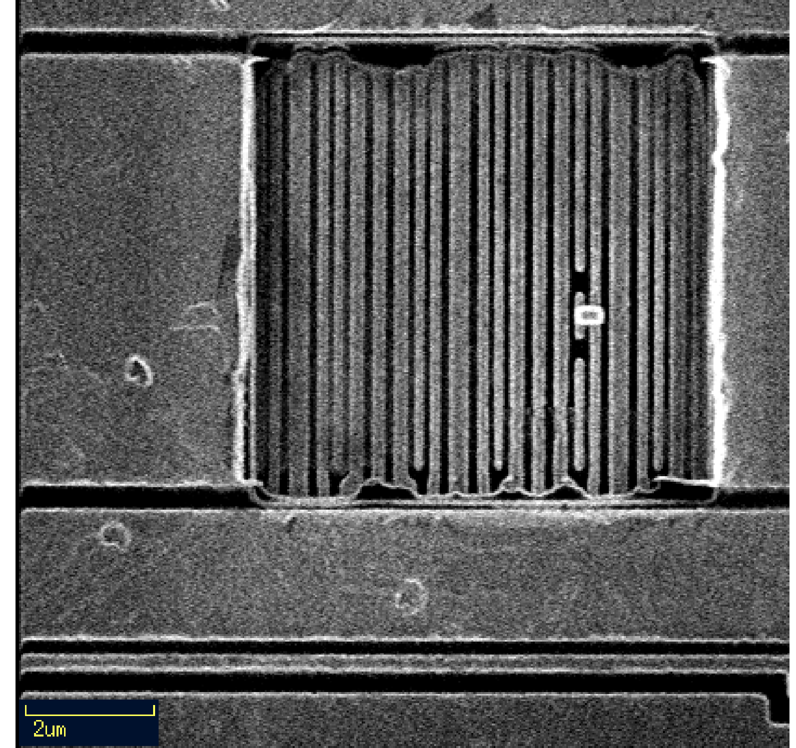
credence

- **Conductor overspray: performance & productivity issues**
  - Performance issues: leakage, added capacitance, & dielectric damage during clean-up
  - Productivity issue: clean-up time
- **Overspray clean-up solutions:**
  - Don't have overspray to begin with
    - none known & not reason for decision
  - Use depo recipes that give minimal overspray
  - Use depo chemistry which cleans up easily
  - Use depo clean-up chemistry which "protects" dielectric



Connect floating M1 trace to adjacent M1 & clean-up





Results:

300 x 200 nm Mo deposit

Re-connection observed

Mo over-spray successfully cleaned

Edit completed without damage to underlying dielectric

Impossible Edits

- **Reconstructive Micro-Surgery**
  - Re-routing traces
  - Circuit knowledge enables re-routing non-critical traces
  - More time consuming but higher success
- **Why an edit is impossible**
  - Spaces between lines are not great enough to work in
- **How:**

1. **Edit from backside**
2. **Find better location not possible or required**
   - Use Layout highlighting to follow net around device, to see if edit could be performed at another site.
3. **Re-route one or more traces to gain area to work in.**
   - Use Layout highlighting to follow close traces around device, to see if these could be edited to open edit site.
     - Grounds & power can often be re-routed
   - Individually edits are possible & probability of success is good.

Conclusions

- Issues:
  - **Top Aluminum metallization**
  - **Blind navigation**
  - **Copper metallizations**
  - **Low-k dielectric**
  - **Conductor overspray clean-up**
  - **Impossible edits**
  -
  -
  -
- Real issue is edit success rate & edit throughput
  1. Performance
  2. Productivity

* Voltage Contrast/Isolation Reference: CR Musil, JL Bartelt, J Melngailis, "Focused Ion Beam Microsurgery for Electronics", *IEEE Electron Device Lett EDL-7* (1986) 285.