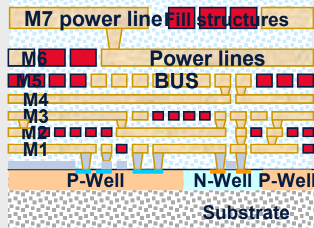
Improvements to support navigation and access in the field of FIB device modification

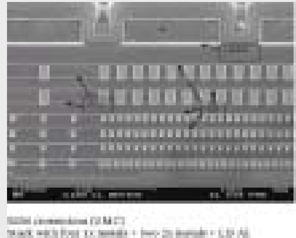
Siegfried Pauthner, Christian Burmer, Jérôme Touzel, Infineon Technologies

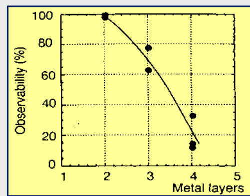
The Focused Ion Beam (FIB) technique is widely established for circuit edit especially for debugging, in-depth characterization or prototyping. Up to now the FIB tools could keep pace with the technology development in some degree, meaning that circuit edit could be done with a reasonable success probability. This will be more and more difficult for the state-of-the-art products and technologies, of course due to the shrinking size of the structures and the increasing number of metal layers used for the wiring, but also because of design features required by the manufacturing lines.

Problems / Issues

Accessibility



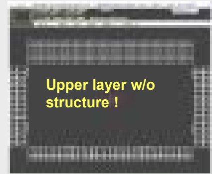




➔ *Edit no longer possible beneath M3 if no design measure !*

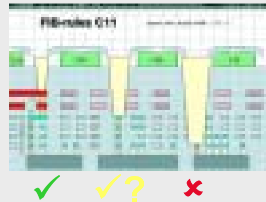
➔ *LB-fills are the main inhibitor, even for the upper metal layers !*

Orientation and Navigation



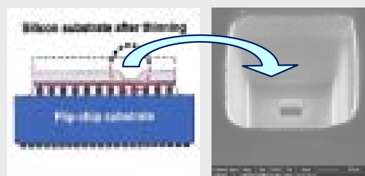
➔ *High likelihood for a "destructive" instead of a constructive edit because of missing or inaccurate navigation !*

Enabling of Edits („Modifiability")



➔ *Exponential decrease of the edit feasibility with the depth of the region of interest !*

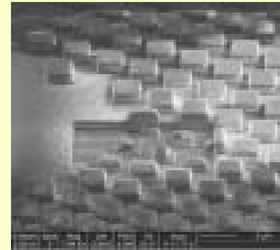
Backside Aspects



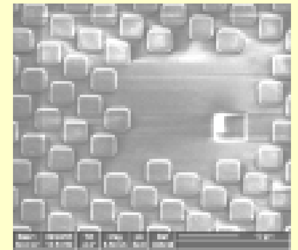
➔ *Basically same topics as for the front side, but turn around time (TAT) 5 x longer (average) !*

Some possible answers

Development Handbook



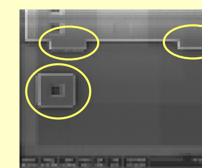
Edit over fill → disturbed edit



Edit in area w/o fill → successful edit

➔ *Reduce - or omit - the fills wherever possible!*

➔ *Implement navigation help (fiducials), e.g. for power grids !*



➔ *Implement E-Beam and / or probing pads for important signals (I/O) if possible up to LB !*

➔ *Implement spare cells (e.g. resistors, …)*

➔ *Implement metal options in upper metal layers !*

➔ *Same topics as above, e.g. back-side probing pad in lowest metal layer !*

Résumé : what you should take in account regarding the future of circuit edit :

- *„First time right" : of course the best way to avoid FIB issues …*
- *But if not, don´t assume that FIB can always save your product !*
- *Use DFM / DFA, for further inputs regarding analysable and „reparable" designs contact the circuit edit team*

Node (nm)	Success rate (%)	TAT (*) (h.)
>350	100	1
180	80	2
130	65	3
90	50?	4
65	20?	5
45	?	?

(*) Front side edit