

New Processes for FIB backside Approach

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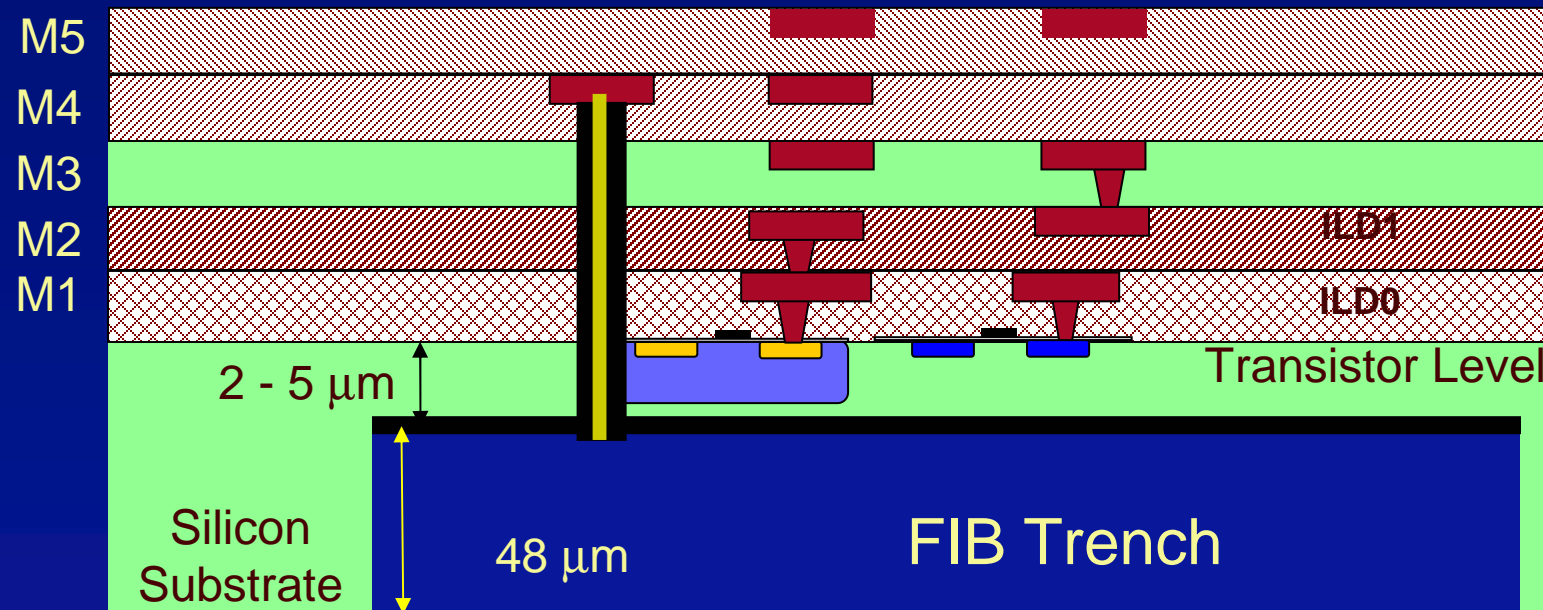
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Introduction

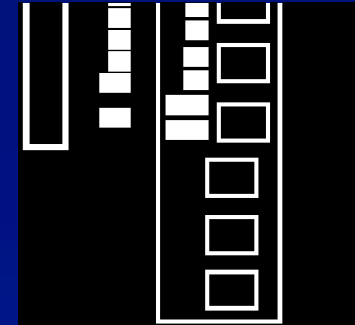


Process Risks of Circuit Edit through Backside:

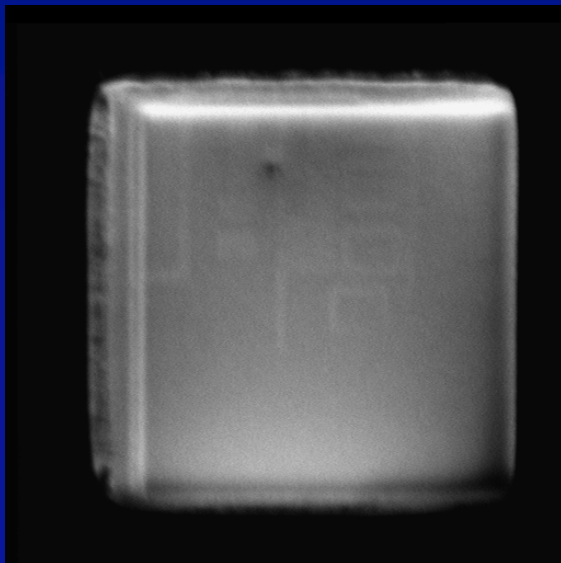
- Trench Flatness
- Endpoint control of trench for active Silicon volume
- Navigation on chip backside

Image Contrast (SE-FIB) of N-Wells Taken from Si-Trench Floor

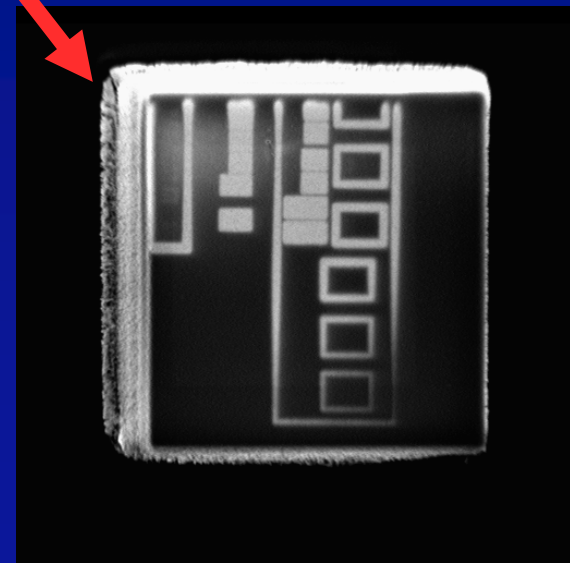
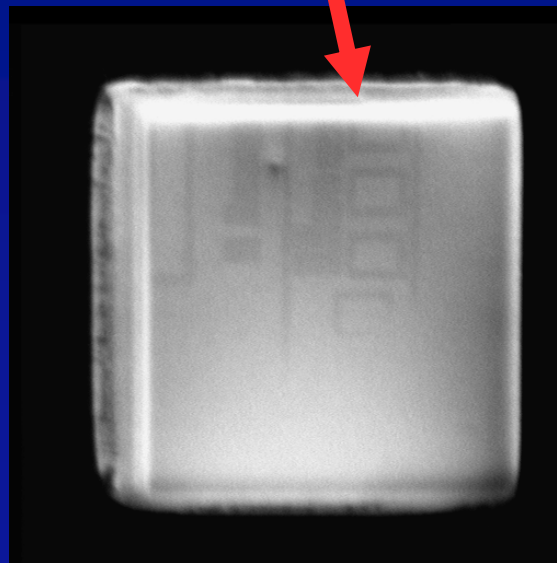
N-well Layout



Transient image
on Silicon
trench floor



Permanent image on
SiO₂ covered surface
SiO₂ thin thick

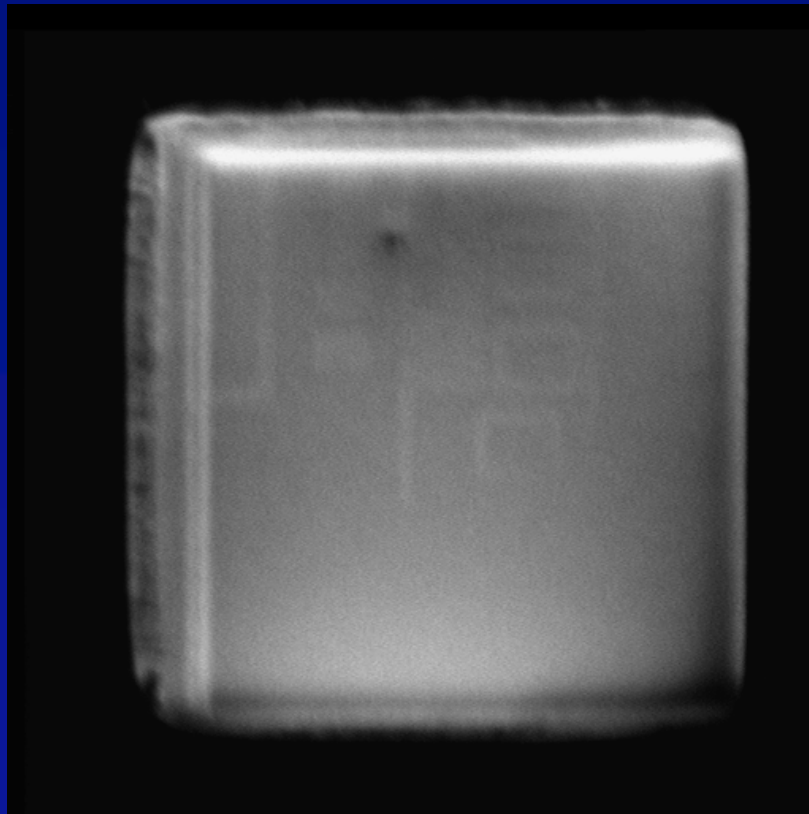


Field of view 182x172mm²

Transient N-well Image Contrast on Silicon Surface

Endpointing contrast variation in FIB-SE image of the trench floor. Parameters for trenching and imaging are 15keV beam energy and 4nA beam current.

The n-wells appear slightly brighter than the p-substrate. Transient image due to XeF_2 trench floor cleanup



Field of view 182x172mm²

Imaging Contrast for Endpoint Control

when n-well space charge overlaps Ga-related space charge and helps compensate positive surface charge

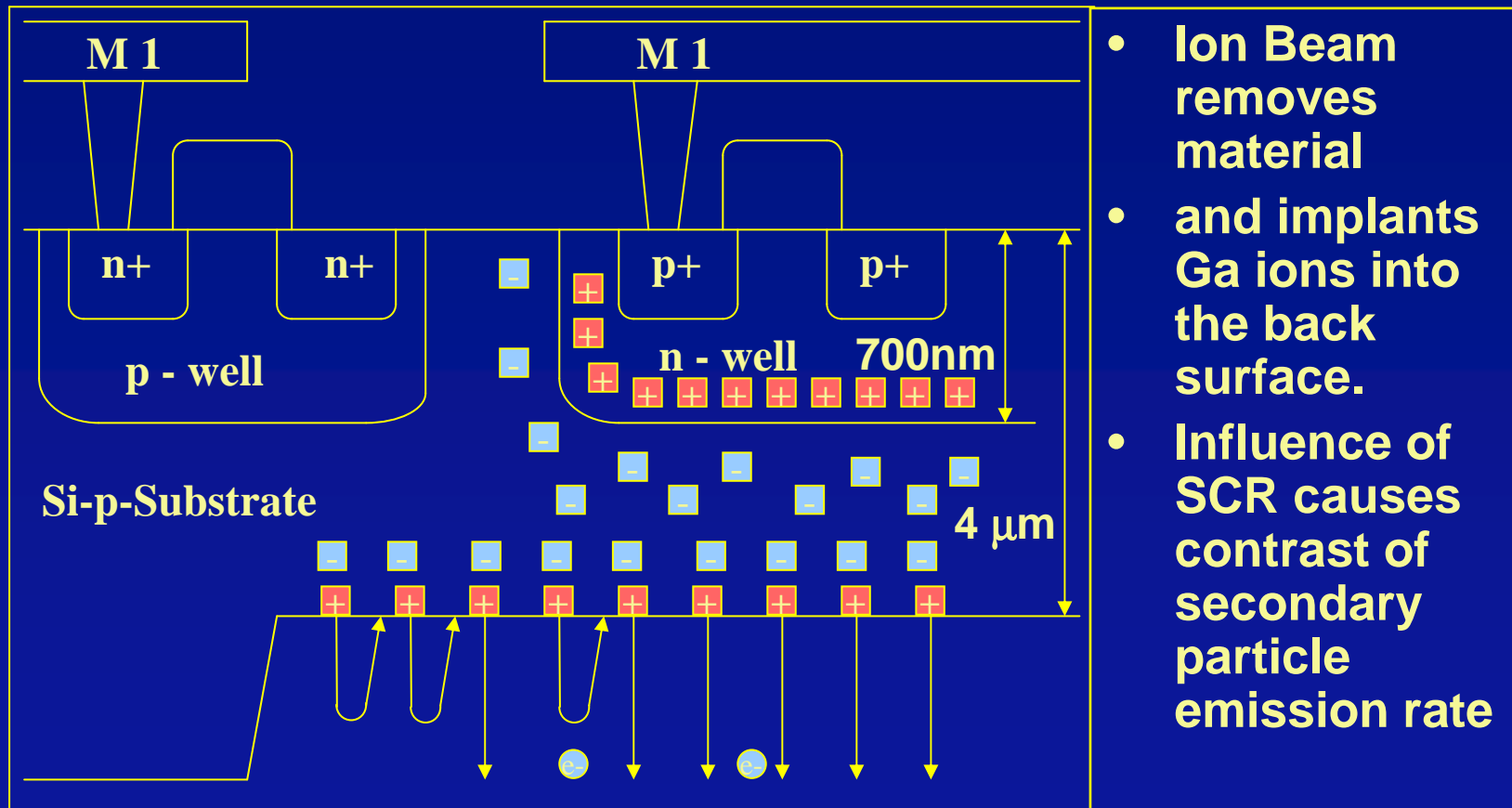
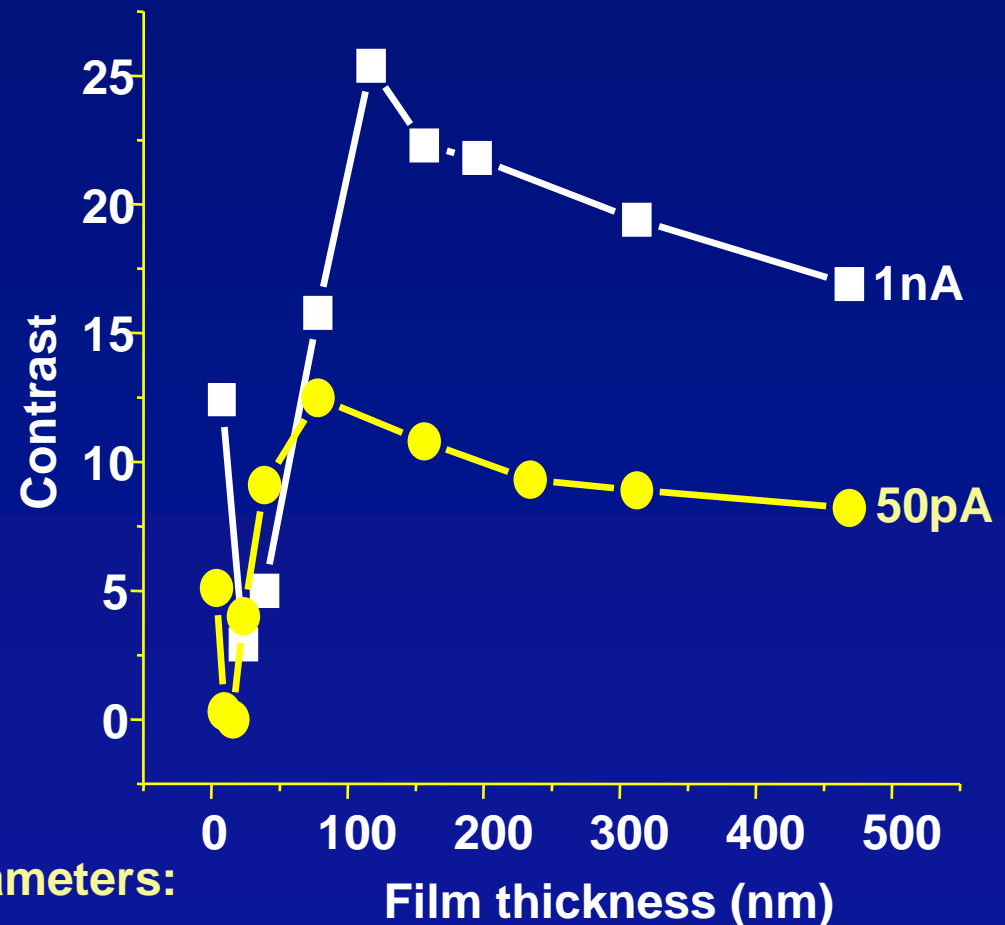


Image Contrast on SiO_x Film Surface

- Contrast variation on the trench floor as a function of SiO_x film thickness for two imaging beam currents.
- At film thicknesses below the contrast minimum, the n-wells appeared dark, while they appeared bright for thicker films.



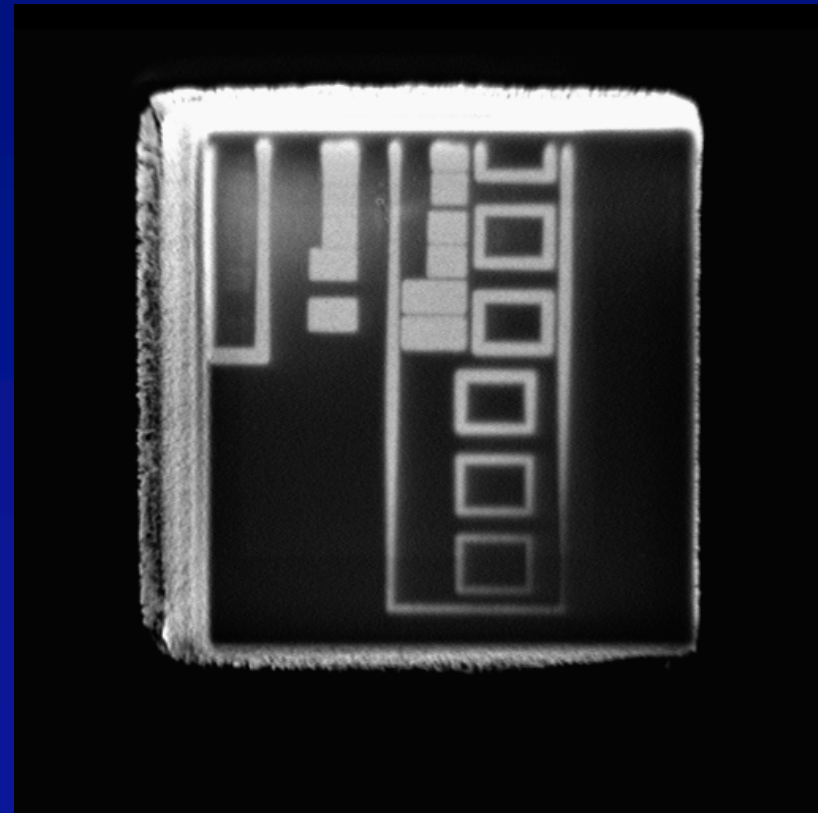
SiO_x deposition parameters:
15keV, 4nA

Imaging parameters: : 30 keV

Permanent Image contrast on Insulator Surface

*Image Contrast after
19min of SiO_x
deposition on the
trench floor (thickness
130nm, 15keV and 4nA
deposition parameters)*

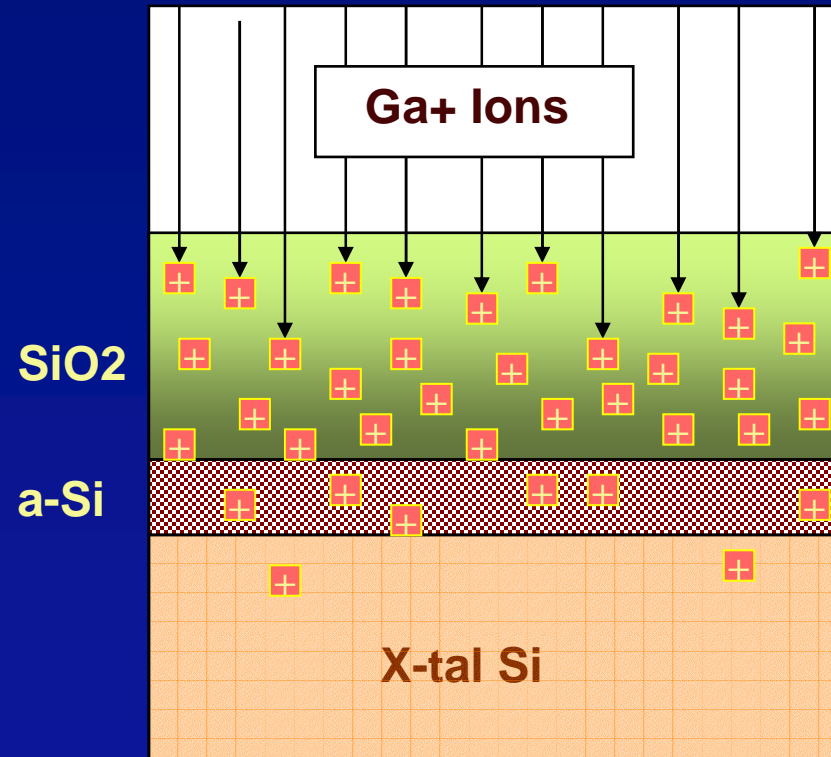
*The n-wells appear much
brighter than the p-
substrate.*



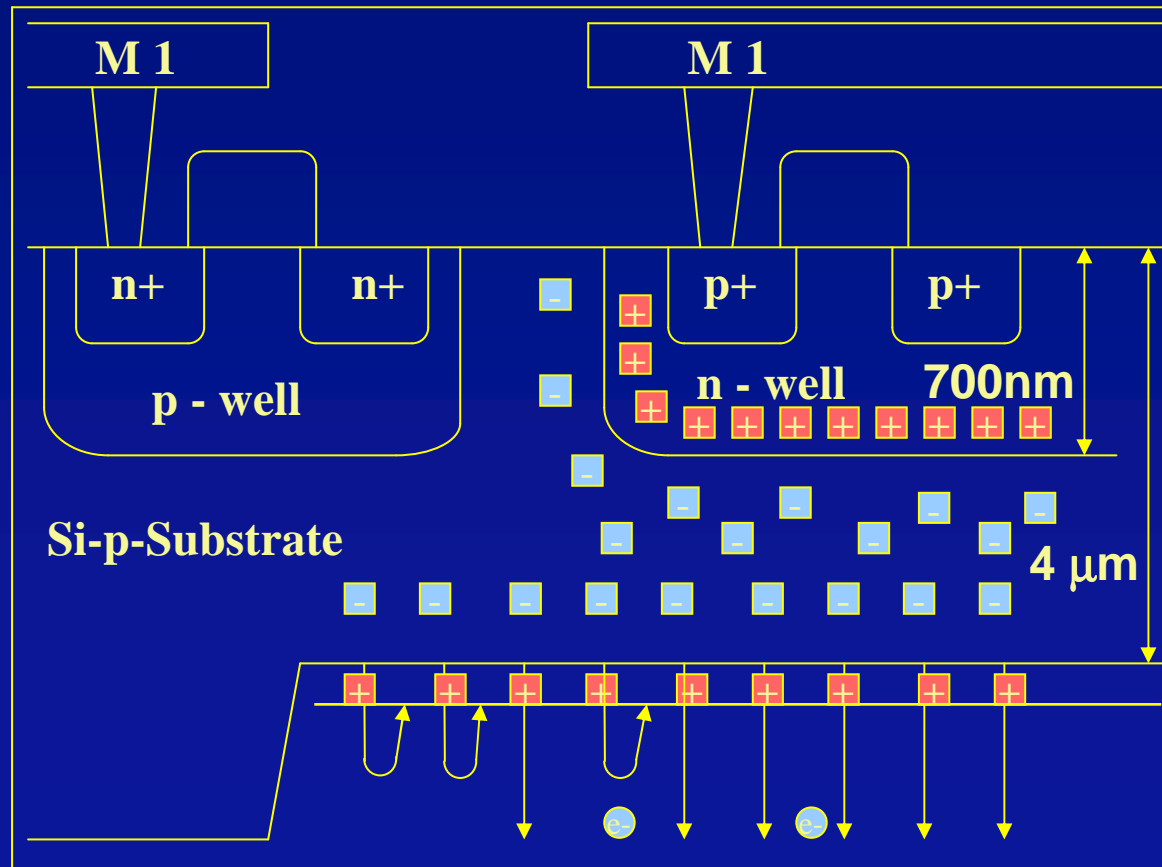
*Imaging parameters are 30keV and 6nA.
Field of view 182x172mm².*

Ga ion Implant at $t_{ox} > 30\text{nm}$

When $t_{ox} > 30\text{nm}$, the Ga ions of the sweep are implanted in oxide layer, creating a space charge similar to the silicon surface case - but more intense and permanent (no removal by XeF_2)



Model for Image Contrast on Insulator Deposition > 30nm



When insulator exceeds thickness of amorphized layer, charges that are built into the oxide permanently create contrast stronger than in transient case

Conclusion

- **At a remaining Silicon thickness of 3-5 μm , a FIB-SE image contrast of the wells occurs**
- **This contrast, although transient, can be used for endpoint detection of the Silicon trench in a circuit edit process through chip backside**
- **The contrast can be made permanent by SiO_x deposition on the trench floor, visualizing the wells for CAD-FIB alignment or analysis purposes**
- **The effects can be understood quantitatively with common semiconductor device models**

Further Projects

- **Parametric Investigation of deposited interconnects on backside topography**
- **Reliability Issues**
- **Edit options on silicon**