FIB Assisted Localisation and Preparation of Gate Oxide Fails

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Physical Failure Analysis
FIB Assisted Localisation and Preparation of Gate Oxide Fails

- Problem Description and Electrical Findings
- Circuit Analysis for FIB Voltage Contrast
- Localisation of Fails with FIB Voltage Contrast
- Preparation of Fails - Uncovering of Gate Oxide
- PFA Findings
- Solving of the Problem
- Summary, Acknowledgement, Questions to be discussed
Problem Description and Electrical Findings

128Mbit DRAM

address pads
## Problem Description and Electrical Findings

### Input Leakage Current of affected Components

3 Address Pads are affected

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Current in nA

Measurements by Ulrich Wende, Infineon DD200 PE D2
Problem Description and Electrical Findings

Schematic of Input Receiver and Transistor Layout

by Mirko Reißmann, Infineon DD 200 PE D5
Problem Description and Electrical Findings

$V_{\text{gate}} - I_{\text{Gate}}$ - Plot of Good and Failing Chips - Gate Oxide Breakdown suspected

by Armand Beyer, Infineon DD 200 PAR
Circuit Analysis for FIB Voltage Contrast

Voltage Contrast Principle

Ion Beam

Secondary Electrons

Substrate

Floating Structure

Grounded Structure
Circuit Analysis for FIB Voltage Contrast

X-section

Top Down

Active area

STI
Circuit Analysis for FIB Voltage Contrast

X-section

Active area

Top Down

gate contact
S/D contact
gate

gate contacts suited for voltage contrast
Circuit Analysis for FIB Voltage Contrast

X-section

Top Down

Metal 0 level suited for voltage contrast
Circuit Analysis for FIB Voltage Contrast

X-section

Top Down

Active area

contact C1
metal 0
gate contact
S/D contact
gate

STI

contacts C1 suited for voltage contrast
Circuit Analysis for FIB Voltage Contrast

X-section

Top Down

- Metal 1 level suited for voltage contrast, but FIB cut necessary
Circuit Analysis for FIB Voltage Contrast

X-section

Active area

S/D contact
gate contact

Top Down

metal 2
contact C2
metal 1
contact C1
metal 0
gate con
S/D con
gate

STI

metal 2 level not suited for voltage contrast
Circuit Analysis for FIB Voltage Contrast

X-section

Active area

Top Down

photoimide
final pass.
metal 2
contact C2
metal 1
contact C1
metal 0
gate contact
S/D contact
gate

STI

Active area
Localisation of Fails with FIB Voltage Contrast

1. Deprocessing down to metal 1 level
   - 1. Removal of photoimide with plasma etch
   - 2. Removal of final passivation with plasma etch
   - 3. Removal of metal 2 with hot phosphoric acid
   - 4. Removal of interlevel dielectric with plasma etch
Localisation of Fails with FIB Voltage Contrast

2. FIB voltage contrast on M1 level

reference
Localisation of Fails with FIB Voltage Contrast

2. FIB voltage contrast on M1 level

reference 1 fail 1
Localisation of Fails with FIB Voltage Contrast

2. FIB voltage contrast on M1 level

reference 2

fail 2
Localisation of Fails with FIB Voltage Contrast

3. FIB voltage contrast on contacts beneath M1 level

Top down milling with FIB

reference

FIB by Peggy Hambsch, Infineon DD 200 PFA
Localisation of Fails with FIB Voltage Contrast

3. FIB voltage contrast on contacts beneath M1 level

Top down milling with FIB

reference

dark contacts - gate is o.k.

fail

bright contacts - gate is leaking
Localisation of Fails with FIB Voltage Contrast

4. FIB voltage contrast on M0 level

Top down milling with FIB

**Reference**
- dark m0 spot - gate is o.k.

**Fail**
- bright m0 spot - gate is leaking

(same voltage contrast at ~10μA and 60nA fails)
Preparation of Fails - Uncovering of Gate Oxide

- gate oxide
- cap nitride
- tungsten silicide
- gate poly Si

substrate

preparation target

STI
Preparation of Fails - Uncovering of Gate Oxide

Classical approach: finger polish

- Time consuming, hard to perform, just one small location per sample

30 s steps on a softpad, just water used

This colour indicates gate poly level
right after having done VC on metal 1 we proceeded with revealing the gc cap nitride with FIB
Preparation of Fails - Uncovering of Gate Oxide

New approach: FIB top down preparation combined with plasma and wet etch

Detailed view of gate conductor
Preparation of Fails - Uncovering of Gate Oxide

New approach: FIB top down preparation combined with plasma and wet etch

Reveal tungsten silicide with plasma etch
Preparation of Fails - Uncovering of Gate Oxide

New approach: FIB top down preparation combined with plasma and wet etch

Reveal gate poly Si with wet etch
Preparation of Fails - Uncovering of Gate Oxide

New approach: FIB top down preparation combined with plasma and wet etch
PFA Findings

SEM image of failing gate oxide

fail 1

Pin hole in gate oxide
PFA Findings

SEM image of failing gate oxide

Pin hole in gate oxide
PFA Findings

SEM image of reference gate oxide

reference 1

Gate oxide o.k.
PFA Findings

SEM image of reference gate oxide

reference 2

Gate oxide o.k.
TEM image shows that critical location for gate oxide breakdown is the edge of AA because of lowest gate oxide thickness.

This corresponds to the SEM findings.

TEM by Lutz Hillmann, Infineon DD 200 PFA
Solving of the Problem

Wafer Distribution of Fails - Contact Etch Tool suspected

XY Scatter Plot from iilh

Legend

- Fail
- Pass

Chips with IILH at least one IILH > 20 nA
Solving of the Problem

C2 contact etch
various experiments with different etch tools and recipes performed

red: failing dies

Tool 1

Tool 2
Fields of plasma etch tools induced high voltages which led to gate oxide breakdown.
Summary (1)

Combination of FIB VC and top down milling at one FIB session saves time, is reproducible and can be performed on several locations of the sample.

Top down polish down to gate poly is time consuming, requires experience and can only be performed on a limited region of the sample.

Not all steps could be performed with FIB top down milling.

Combination with dry/wet etch preparation is necessary to gain uniformity.
**Summary (2)**

Gate oxide pinholes are hard to detect, high resolution SEM is required

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<th>Electrically Failing Gates</th>
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<td>60% showed pinholes</td>
<td>All were clean</td>
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<td>20% showed probable pinholes</td>
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<td>20% were clean</td>
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VC showed same images in a wide range of fail current from 10µA down to 60 nA
Acknowledgement

I want to thank my colleagues at Infineon Dresden for their contributions to this paper:

Dr. Ulrich Wende
Dr. Armand Beyer
Peggy Hambsch
Dr. Lutz Hillmann
Dr. Matthias Junack
Dr. Oliver Pyper
Mirko Reißmann
Questions to be discussed

1. Your questions
2. Influence of ion incident angle to sputter rate and uniformity
3. Gas assisted etch for top down milling
4. Which minimum fail current is necessary to get a clear voltage contrast