Novel FIB-based sample preparation technique for TEM analysis of ultra-thin gate oxide breakdown

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Outline

- Properties of soft breakdown
- Microscopy and sample preparation challenges
- New approach
- First results
- Summary and Outlook
Theory of dielectric breakdown

Breakdown statistics

trap percolation model

Ref.: Degraeve et.al. IEDM 1995
**Microscopy challenge**

- sBD site ≈ 1-10 nm
- visible structure change?
- TEM provides high-resolution non-destructive observation
- TEM lamella preparation
- lamella thickness 100 nm
Horizontal lamella

Ar ion beam thinning

pre-thinned chip

useful area
Horizontal lamella - II

SAPTEM

- thinning of chip to \( \approx 30 \, \mu m \)

- polish (vertically to chip surface) to \( \approx 25 \, \mu m \) distance of the site

- bulk FIB cut

- planar FIB cut

Subramanian et al., Motorola, ISTFA 1998
Horizontal lamella - III

- irregularities of the polysilicon gate material visible in TEM image

- poly-silicon
- gate oxide
- single crystalline silicon
Vertical TEM lamella using the FIB

- TEM lamella thickness
  \( \approx 100 \text{ nm} \)

- Defect localisation accuracy
  \( \pm 500 \text{ nm} \)

- 90% probability to lose the damage site
## TEM lamella preparation methods

<table>
<thead>
<tr>
<th></th>
<th>Ar-ion</th>
<th>vertical FIB lamella</th>
<th>SAPTEM</th>
<th>?</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>surface quality</strong></td>
<td>excellent</td>
<td>moderate</td>
<td>moderate</td>
<td>at least moderate</td>
</tr>
<tr>
<td><strong>other effects</strong></td>
<td>none</td>
<td>none</td>
<td>polysilicon grains</td>
<td>none</td>
</tr>
<tr>
<td>reducing sBD visibility</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<tr>
<td><strong>chance to hit point of interest</strong></td>
<td>0 -1 %</td>
<td>10 %</td>
<td>90 %</td>
<td>90 %</td>
</tr>
</tbody>
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New approach

lamella thickness

100 nm

gate oxide

gate
Problems to be solved

- is TEM still possible for lamella thickness $> 100 \text{ nm}$?

- can the FIB cuts be positioned accurately enough?
TEM of thick lamella

gate oxide

TEM beam

gate oxide layer

500 nm

500 nm

t = 100 nm

t = 500 nm
FIB cut positioning

ion beam

electron beam

lamella

gate

100 nm
FIB cut positioning - II

contact

ion beam

gate

electron beam

100 nm

lamella
Lamella preparation
First results

lamella thickness 400 - 500 nm
Hard gate oxide breakdown

gateoxide $t_{ox} = 5$ nm

substrate

damage area

polysilicon - silicide gate

original structure

amorphous structure

amorphous silicon

contact (W-plug)

STI

0.2 µm

0.5 µm
Required lamella thickness for future technologies

Perspective
Summary

- soft gate oxide breakdown microscopy challenge
- TEM most promising microscopy technique
- drawbacks of existing sample preparation methods
- demonstration of a new TEM lamella preparation approach providing
  - good surface quality
  - good visibility of the gate oxide
  - high chance to get the point of interest into lamella
  - less complex than SAPTEM
  - acceptable image quality in spite of the high lamella thickness (demonstrated for channel length of 250 nm)
  - lamella thickness reduces for future technologies